Anybus® CompactCom B40-1

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Table of Contents

1   Preface

1.1   About this Document

This document is intended to provide a good understanding of how to use the Anybus CompactCom B40-1.

The reader of this document is expected to be familiar with hardware design and communication systems in general. For additional information, documentation, support etc., please visit the support website at www.anybus.com/support.

1.2   Related Documents

Document	Author	Document ID
Anybus CompactCom 40 Software Design Guide	HMS	HMSI-216-125
Anybus CompactCom 40 Network Guides	HMS	
Anybus CompactCom Host Application Implementation Guide	HMS	HMSI-27-334

1.3   Document history

Version	Date	Description
1.23	2015-09-03	Last FM version.
2.0	2016-03-10	Moved from FM to XML Misc. updates
2.1	2016-12-07	Added information for Anybus CompactCom B40 CC-Link IE Field Minor corrections and updates
3.0	2017-09-12	Added content to make the design guide independent of the M40 HWDG Added new example schematics Added BACnet/IP
3.1	2018-03-09	Updated section on DIP1 and DIP2 usage Added section on EMC Misc corrections
3.2	2018-05-25	Corrected pinnings for 8-bit parallel Misc corrections
3.3	2018-10-23	Minor corrections
3.4	2019-02-27	Updated for CANopen release Rebranded

1.4 Document Conventions

Ordered lists are used for instructions that must be carried out in sequence:

1. First do this

2. Then do this

Unordered (bulleted) lists are used for:

• Itemized information

• Instructions that can be carried out in any order

...and for action-result type instructions:

► This action...

  → leads to this result

Bold typeface indicates interactive parts such as connectors and switches on the hardware, or menus and buttons in a graphical user interface.

```
Monospaced text is used to indicate program code and other
kinds of data input/output such as configuration scripts.
```

This is a cross-reference within this document: *Document Conventions, p. 4*

This is an external link (URL): www.hms-networks.com

$\mathbf{\hat{1}}$ *This is additional information which may facilitate installation and/or operation.*

! This instruction must be followed to avoid a risk of reduced functionality and/or damage to the equipment, or to avoid a network security risk.

⚠ Caution
This instruction must be followed to avoid a risk of personal injury.

⚠ WARNING
This instruction must be followed to avoid a risk of death or serious injury.

1.5 Document Specific Conventions

• The terms "Anybus" or "module" refers to the Anybus CompactCom module.

• The terms "host" or "host application" refer to the device that hosts the Anybus.

• Hexadecimal values are written in the format NNNNh or 0xNNNN, where NNNN is the hexadecimal value.

• A byte always consists of 8 bits.

• All dimensions in this document have a tolerance of ±0.10 mm unless otherwise stated.

• Outputs are TTL compliant unless otherwise stated.

• Signals which are "pulled to GND" are connected to GND via a resistor.

• Signals which are "pulled to 3V3" are connected to 3V3 via a resistor.

• Signals which are "tied to GND" are directly connected to GND,

• Signals which are "tied to 3V3" are directly connected to 3V3.

1.5.1   PIN Types

The pin types of the connectors are defined in the table below. The pin type may be different depending on which mode is used.

Pin type	Definition
I	Input
O	Output
I/O	Input/Output (bidirectional)
OD	Open Drain
Power	Pin connected directly to module power supply, GND or 3V3

1.6   Trademark Information

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2   About the Anybus CompactCom B40-1

2.1   General Information

The Anybus CompactCom B40-1 concept is developed for applications where the standard Anybus CompactCom M40 cannot be used. The brick consists of a board with network connectivity functionality, where the customer provides the physical network interface, including network connectors. There are also available interface boards for several networks, providing network connectors and physical interface.

All Anybus CompactCom B40-1 share footprint and electrical interface. The brick has two connectors that provides communication with the host application board. The host application connector provides an interface between the host application and the brick, while the network connector provides network access. This enables full Anybus CompactCom functionality for all applications without loss of network compatibility or environmental characteristics.

All dimensions expressed in this document are stated in millimeters and have a tolerance of ±0.10 mm unless stated otherwise.

For general information about the Anybus CompactCom 40 platform, consult the Anybus CompactCom 40 Software Design Guide.

> **!** This a class A product. In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate measures.
>
> This product contains ESD (Electrostatic Discharge) sensitive parts that may be damaged if ESD control procedures are not followed. Static control precautions are required when handling the product. Failure to observe this may cause damage to the product.

2.2   Features

- Hardware support for triple buffered process data, which increases performance

- Supports synchronization for selected industrial networks

- Black channel interface, offering a transparent channel for safety communication for selected networks

- Low latency

- Integrated protocol stack handling (where applicable)

- Control pins for status indications according to each network standard (where applicable)

- Separate network connector boards available

- Firmware upgradable (FLASH technology)

- 3.3 V design

- 8-bit and 16-bit parallel modes

- SPI mode

- Shift register mode

- UART/Serial mode

- Transparent Ethernet functionality

- Precompliance tested for network conformance (where applicable).

- Precompliance tested for CE & UL. Contact HMS Industrial Networks for further information.

> **!** All Anybus CompactCom B40-1 will be precertified for network conformance. This is done to ensure that the final product can be certified, but it does not necessarily mean that the final product does not require recertification. Contact HMS Industrial Networks for further information.

3 Host Interface

This chapter describes the low level properties of the Anybus CompactCom interface.

3.1 Overview

The Anybus CompactCom has five different host communication interfaces, corresponding to different operating modes. The figure below illustrates the basic properties of these interfaces as well as various I/O and control signals, and how they relate to the host application.
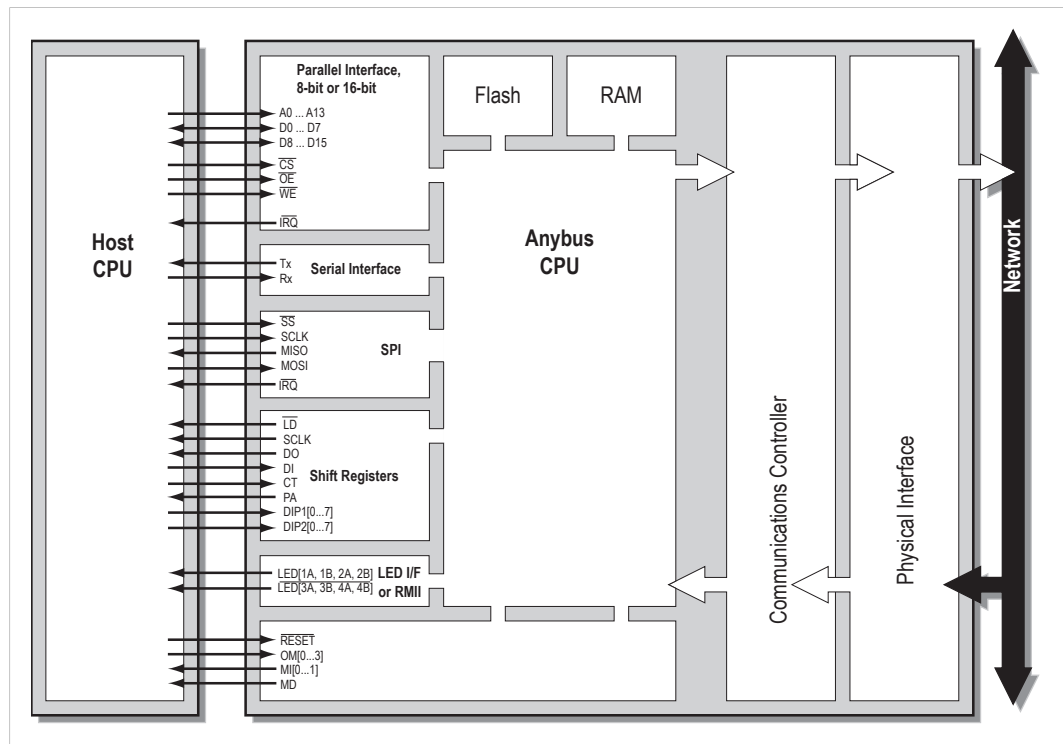
Fig. 1

Please note that only one communication interface at a time is available. Which one is decided at startup.

3.1.1 Parallel Interface, 8-bit or 16-bit

From an external point of view, the parallel interface is a common 8-bit or 16-bit parallel slave port interface, which can easily be incorporated into any microprocessor based system that has an external address/data bus. Generally, implementing this type of interface is comparable to implementing an 8-bit or 16-bit wide SRAM. Additionally, the parallel interface features an interrupt request line, allowing the host application to service the module only when actually needed.

3.1.2 SPI

The Serial Peripheral Interface (SPI) is a synchronous serial link. It operates in full duplex mode and devices communicate in master/slave mode where the Anybus CompactCom modules always act as slaves. The interface can provide much higher performance than the serial interface, but not as high as the parallel interface.

3.1.3   Stand-Alone Shift Register Interface

In this mode the Anybus CompactCom B40-1 operates stand-alone, with no host processor. Process data is communicated to the shift registers on the host.

3.1.4   Serial Interface (UART)

The serial interface is provided for backward compatibility with the Anybus CompactCom 30. The interface is event based, and has lower performance than the SPI and parallel modes. For more information about the serial interface, see the Anybus CompactCom Hardware Design Guide for the 30 series.

Please note that the Anybus CompactCom B40-1 is not backward compatible to the Anybus CompactCom B30 hardware wise.

3.1.5   LED Interface

The status of the network LEDs is available as follows:

- As LED output signals on the network interface connector. These signals are able to drive a LED directly and are available for all networks and operating modes. (Recommended)

- As LED output signals on the host interface connector for all operating modes except 16-bit parallel mode. These signals are not able to drive a LED directly.

- In the LED status register for all modes, see Anybus CompactCom 40 Software Design guide for more information.

3.1.6   Reduced Media-Independent Interface (RMII)

This interface is used for Transparent Ethernet, where Industrial Ethernet communication is handled by the Anybus CompactCom and other Ethernet communication is routed to the host application. 16–bit parallel mode and the LED Interface signals are not available in the host application connector when Transparent Ethernet is enabled. The LED signals are still available on the network connector of the Anybus CompactCom B40-1.

See *RMII — Reduced Media-Independent Interface, p. 17* for mor information.

3.2   Host Application Connector

The host application connector provides an interface between the host application and the
Anybus CompactCom B40-1.
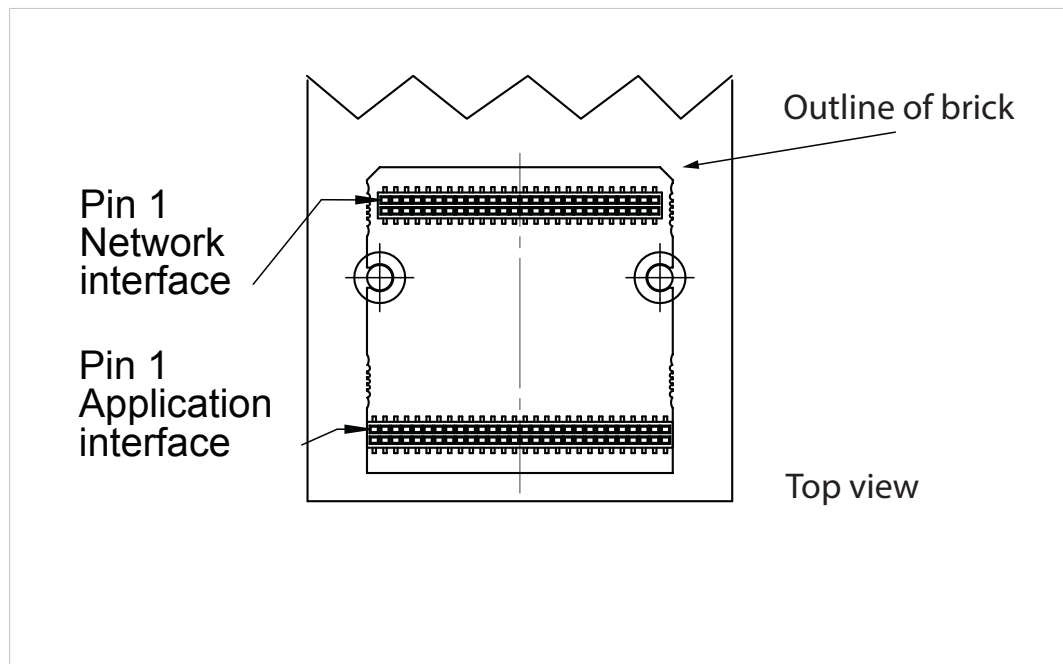
Fig. 2

The connector is implemented by a standard 1.27 mm 56 pin header surface mounted to the
bottom side of the PCB.
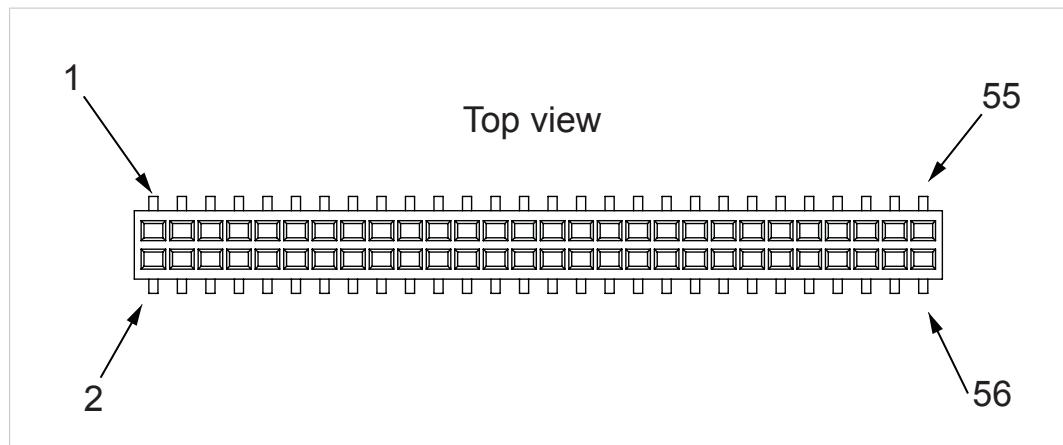
Fig. 3

The pictures shows the pinning of the mating connector on the host application seen from the
top.

```
                   GND  2  ☐  ☐  1   3V3
        A0/WEH/DIP1_0  4  ☐  ☐  3   RESET
          A2/DIP1_2  6  ☐  ☐  5   A1/DIP1_1
                   GND  8  ☐  ☐  7   A3/DIP1_3
          A5/DIP1_5 10  ☐  ☐  9   A4/DIP1_4
          A7/DIP1_7 12  ☐  ☐  11  A6/DIP1_6
                  GND 14  ☐  ☐  13  A8/LD/SS
        A10/DO/MISO 16  ☐  ☐  15  A9/SCLK
                  GND 18  ☐  ☐  17  A11/DI/MOSI
         A13/ASI_TX 20  ☐  ☐  19  A12/ASI_RX
          D6/DIP2_6 22  ☐  ☐  21  D7/DIP2_7
                  GND 24  ☐  ☐  23  D5/DIP2_5
          D3/DIP2_3 26  ☐  ☐  25  D4/DIP2_4
                  GND 28  ☐  ☐  27  D2/DIP2_2
                  MD0 30  ☐  ☐  29  D1/DIP2_1
                  OM0 32  ☐  ☐  31  D0/DIP2_0
                  GND 34  ☐  ☐  33  OM1
                   CS 36  ☐  ☐  35  OM2
               IRQ/PA 38  ☐  ☐  37  WE/WEL/CT
                  GND 40  ☐  ☐  39  OE
          LED4B/D14 42  ☐  ☐  41  LED4A/D15
                  GND 44  ☐  ☐  43  LED3A/D13
          LED2A/D11 46  ☐  ☐  45  LED3B/D12
           LED1A/D9 48  ☐  ☐  47  LED2B/D10
                  GND 50  ☐  ☐  49  LED1B/D8
      TX/ASI_TX/OM3 52  ☐  ☐  51  RX/ASI_RX
           MI0/SYNC 54  ☐  ☐  53  MI1
                  GND 56  ☐  ☐  55  3V3
```

Fig. 4

See *Pin Overview, p. 12* for information on how each pin is used in the different modes.

3.2.1 Pin Overview

Depending on operating mode, the pins have different names and different functionality. Presented below is an overview of all pins except GND and 3V3.

The pin types of the connector are defined in *PIN Types, p. 5*. The pin type may be different depending on which mode is used.

> ⓘ *The ASI (Anybus Safety Interface) signals are used to connect a safety module to the safety interface of an Anybus CompactCom 40-series module.*

> ❗ **Note**: The pin numbers of the Anybus CompactCom B40 (brick) host application connector are different from those of the Anybus CompactCom M40 (module) host application connector.

Pin	Signal Name					Type	Notes
	Serial Mode	SPI Mode	8-bit Mode	16-bit Mode	Shift Register Mode		
4	DIP1_0	DIP1_0	A0	$\overline{\text{WEH}}$	DIP1_0	I	
5	DIP1_1	DIP1_1	A1	A1	DIP1_1	I	
6	DIP1_2	DIP1_2	A2	A2	DIP1_2	I	
7	DIP1_3	DIP1_3	A3	A3	DIP1_3	I	
9	DIP1_4	DIP1_4	A4	A4	DIP1_4	I	
10	DIP1_5	DIP1_5	A5	A5	DIP1_5	I	
11	DIP1_6	DIP1_6	A6	A6	DIP1_6	I	
12	DIP1_7	DIP1_7	A7	A7	DIP1_7	I	
13		$\overline{\text{SS}}$	A8	A8	$\overline{\text{LD}}$	I/O	
15		SCLK	A9	A9	SCLK	O, I	
16		MISO	A10	A10	DO	O, I	
17		MOSI	A11	A11	DI	I	
19	ASI RX		A12	A12		I	
20	ASI TX		A13	A13		O, I	
31	DIP2_0	DIP2_0	D0	D0	DIP2_0	I, I/O	
29	DIP2_1	DIP2_1	D1	D1	DIP2_1	I, I/O	
27	DIP2_2	DIP2_2	D2	D2	DIP2_2	I, I/O	
26	DIP2_3	DIP2_3	D3	D3	DIP2_3	I, I/O	
25	DIP2_4	DIP2_4	D4	D4	DIP2_4	I, I/O	
23	DIP2_5	DIP2_5	D5	D5	DIP2_5	I, I/O	
22	DIP2_6	DIP2_6	D6	D6	DIP2_6	I, I/O	
21	DIP2_7	DIP2_7	D7	D7	DIP2_7	I, I/O	
49	LED1B	LED1B	LED1B	D8	LED1B	O, I/O	In modules supporting RMII, these pins are used for the RMII interface when this has been activated, see *RMII — Reduced Media-Independent Interface, p. 17*.
48	LED1A	LED1A	LED1A	D9	LED1A	O, I/O	
47	LED2B	LED2B	LED2B	D10	LED2B	O, I/O	
46	LED2A	LED2A	LED2A	D11	LED2A	O, I/O	
45	$\overline{\text{LED3B}}$	$\overline{\text{LED3B}}$	$\overline{\text{LED3B}}$	D12	$\overline{\text{LED3B}}$	OD, I/O	
43	$\overline{\text{LED3A}}$	$\overline{\text{LED3A}}$	$\overline{\text{LED3A}}$	D13	$\overline{\text{LED3A}}$	OD, I/O	
42	$\overline{\text{LED4B}}$	$\overline{\text{LED4B}}$	$\overline{\text{LED4B}}$	D14	$\overline{\text{LED4B}}$	O, I/O	
41	$\overline{\text{LED4A}}$	$\overline{\text{LED4A}}$	$\overline{\text{LED4A}}$	D15	$\overline{\text{LED4A}}$	O, I/O	
37			$\overline{\text{WE}}$	$\overline{\text{WEL}}$	CT	I	
39			$\overline{\text{OE}}$	$\overline{\text{OE}}$		I	
36			$\overline{\text{CS}}$	$\overline{\text{CS}}$		I	
38		$\overline{\text{IRQ}}$	$\overline{\text{IRQ}}$	$\overline{\text{IRQ}}$	PA	O	

Pin	Signal Name					Type	Notes
	Serial Mode	SPI Mode	8-bit Mode	16-bit Mode	Shift Register Mode		
51	RX	ASI RX	ASI RX	ASI RX	ASI RX	I	
52	TX / OM3	ASI TX / OM3	ASI TX / OM3	ASI TX / OM3	ASI TX / OM3	I/O	Strapping input with internal weak pull-up during powerup. To configure OM3, use an external pull-up/pull-down of 1.0 to 2.2 kΩ. The pin changes to output after powerup
32	OM0	OM0	OM0	OM0	OM0	I	
33	OM1	OM1	OM1	OM1	OM1	I	
35	OM2	OM2	OM2	OM2	OM2	I	
54	MI0	MI0/SYNC	MI0/SYNC	MI0/SYNC	MI0/SYNC	O	Low at power-up and before reset release.
53	MI1	MI1	MI1	MI1	MI1	O	Tied to 3V
30	MD0	MD0	MD0	MD0	MD0	O	Tied to GND
3	RESET	RESET	RESET	RESET	RESET	I	

3.2.2 Power Supply Pins

Signal	Type	Pin	Description
GND	Power	2, 8, 14, 18, 24, 28, 34, 40, 44, 50, 56	Ground Power and signal ground reference.
3V3	Power	1, 55	3.3 V power supply.

3.2.3 LED Interface / D8–D15 (Data Bus)

Signal Name	Pin Type	Pin	Description, LED Interface	Description, Data Bus
LED1A / D9	O / I/O	48	LED 1 Indication A • Green	D9 Data Bus • "D9" in 16-bit parallel mode.
LED1B / D8	O / I/O	49	LED 1 Indication B • Red	D8 Data Bus • "D8" in 16-bit parallel mode.
LED2A / D11	O / I/O	46	LED 2 Indication A • Green	D11 Data Bus • "D11" in 16-bit parallel mode.
LED2B / D10	O / I/O	47	LED 2 Indication B • Red	D10 Data Bus • "D10" in 16-bit parallel mode.
LED3A / D13	OD / I/O	43	LED 3 Indication A • Green • Mainly used for link/ activity on network port 1 on the Ethernet modules. Pin is open-drain to maintain backward compatibility with existing applications, where this pin may be tied to GND.	D13 Data Bus • "D13" in 16-bit parallel mode.
LED3B / D12	OD / I/O	45	LED 3 Indication B • Yellow or red, depending on network • Mainly used for link/ activity on network port 1 on the Ethernet modules (yellow). Pin is open-drain to maintain backward compatibility with existing applications, where this pin may be tied to GND.	D12 Data Bus • "D12" in 16-bit parallel mode.
LED4A / D15	O / I/O	41	LED 4 Indication A • Green • Mainly used for link/ activity on network port 2 on the Ethernet modules.	D15 Data Bus • "D15" in 16-bit parallel mode.
LED4B / D14	O / I/O	42	LED 4 Indication B • Yellow or red, depending on network • Mainly used for link/ activity on network port 2 on the Ethernet modules (yellow)	D14 Data Bus • "D14" in 16-bit parallel mode.

ℹ *The LED signals are also available on the network connector as active high push/pull signals. Those signals are easier to use for LEDs.*

3.2.4 Settings / Sync

Signal Name	Type	Pin	Description
OM0 OM1 OM2 OM3 (ASI TX) (TX)	I I I I (Used as OM3 during power up)	32 33 35 52	**Operating Mode** Used to select interface and baud rate, see below.
MI0 / SYNC MI1	O O	54 53	**Module Identification** MI0 and MI1 can be used by the host application to determine what type of Anybus CompactCom that is connected. **SYNC** On networks that support synchronous communication, a periodic synchronization pulse is provided on the SYNC output. The SYNC pulse is also available as a maskable interrupt using the IRQ signal.
MD0	O	30	**Module Detection** This signal can be used by the host application to determine that an Anybus CompactCom is inserted into the slot, see *Module Detection, p. 16*. The signal is connected directly to GND on the Anybus CompactCom.
ASI RX ASI TX	I O	51 52 UART opera-tion: 19 20	**Black Channel Communication** These signals can be connected to a safety module, e.g. to IXXAT Safe T100 to provide a safe channel for black channel communication If not used, pin 51 (for UART operation pin 19) should be pulled to 3V3.
RX TX	I O	51 52	**Serial Communications Signals**

Operating Modes

These inputs select the interface that should be used to exchange data (SPI, stand-alone shift register, parallel or serial) and, if the serial interface option is used, the operating baud rate. The state of these signals is sampled once during startup, i.e. any changes require a reset in order to have effect.

OM3	OM2	OM1	OM0	Operating Mode
LOW	LOW	LOW	LOW	Reserved
LOW	LOW	LOW	HIGH	SPI
LOW	LOW	HIGH	LOW	Stand-alone shift register
LOW	LOW	HIGH	HIGH	Reserved
LOW	HIGH	LOW	LOW	Reserved
LOW	HIGH	LOW	HIGH	Reserved
LOW	HIGH	HIGH	LOW	Reserved
LOW	HIGH	HIGH	HIGH	16-bit parallel
HIGH	LOW	LOW	LOW	8-bit parallel
HIGH	LOW	LOW	HIGH	Serial 19.2 kbps
HIGH	LOW	HIGH	LOW	Serial 57.6 kbps
HIGH	LOW	HIGH	HIGH	Serial 115.2 kbps
HIGH	HIGH	LOW	LOW	Serial 625 kbps
HIGH	HIGH	LOW	HIGH	Reserved
HIGH	HIGH	HIGH	LOW	Reserved
HIGH	HIGH	HIGH	HIGH	Service Mode

LOW = V_{IL}

HIGH = V_{IH}

> ⓘ *These signals must be stable prior to releasing the RESET signal. Failure to observe this may result in faulty behavior.*

Module Detection

This signal is internally connected to GND, and can be used by the host application to detect whether a module is present or not. When connecting an external pull-up resistor, a low signal indicates that a module is present.

If not used, leave this signal unconnected.

Module Identification

These signals indicate which type of module that is connected. It is recommended to check the state of these signals before accessing the module.

MI1	MI0	Module Type
LOW	LOW	Active Anybus CompactCom 30
LOW	HIGH	Passive Anybus CompactCom
HIGH	LOW	Active Anybus CompactCom 40
HIGH	HIGH	Customer specific

LOW = V_{OL}

HIGH = V_{OH}

> ⓘ *On modules supporting "SYNC", MI0 is used as a SYNC signal during operation. MI0 should only be sampled by the application during the time period from power up to the end of SETUP state.*

3.2.5   RMII — Reduced Media-Independent Interface

In RMII enabled modules, the pins described in the table below are used for the RMII communication. They are set to tristate during startup, making it impossilbe to indicate e.g. exception during setup. When setup is complete, they are set to inputs/outputs according to the selected mode. See Anybus CompactCom 40 Software Design Guide for more information on mode selection.

> ❗ The 16-bit parallel mode can not be used when RMII is enabled
>
> LED status will not be available when RMII is enabled.

Pin	Signal Name	Type	Notes
49	RXD0	O	-
48	RXD1	O	-
47	RXDV	O	-
46		I	Not used (connect to external pull-down)
45	TXD0	I	-
43	TXD1	I	-
42	TXEN	I	-
41	CLK	I	-

3.2.6   IRQ (Interrupt Request)

Signal Name	Pin Type	Pin	Description
$\overline{\text{IRQ}}$	O	38	**Interrupt Request** Active low interrupt signal.

The use of this signal is optional but highly recommended. Even if the host application lacks interrupt capabilities, it is recommended to connect this signal to an input port to simplify software design.

This signal must be pulled to 3V3 on the host application side to prevent spurious interrupts during startup.

3.2.7 RESET (Reset Input)

Signal Name	Pin Type	Pin	Description
$\overline{\text{RESET}}$	I	3	**Reset** Used to reset the module.

The master reset input is active low. It must be connected to a host application controllable output pin in order to handle the power up sequence, voltage deviations and to be able to support network reset requests. If the brick is used in stand-alone mode, with no host processor, a separate reset circuit can be used, see *Reset Circuit Example, p. 36*.

The brick does not feature any internal reset regulation. To establish a reliable interface, the host application is solely responsible for resetting the module when the supply voltage is outside the specified range.

Power Up
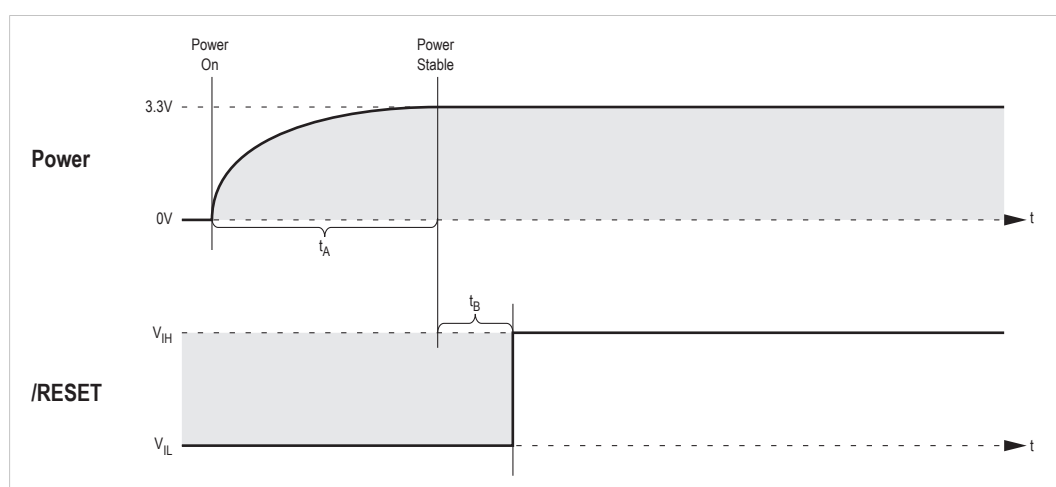
Fig. 5

Powerup time limits are given in the table below:

Symbol	Min.	Max.	Definition
t_A	-	-	Time until the power supply is stable after power-on; the duration depends on the power supply design of the host application and is thus beyond the scope of this document.
t_B	1 ms	-	Safety margin.

Restart

The reset pulse duration must be at least 10 µs in order for the NP40 to properly recognize a
reset.
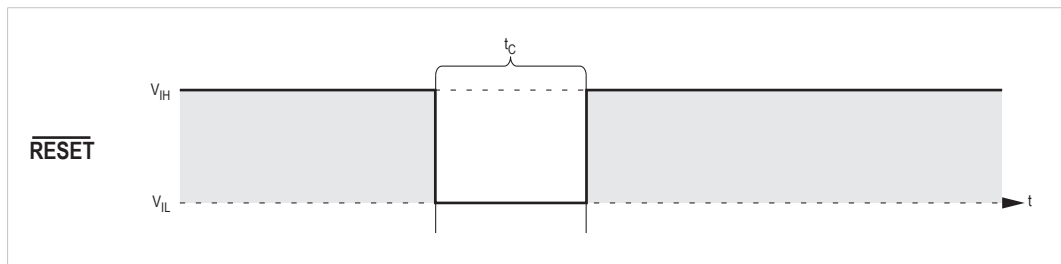
Fig. 6

Symbol	Min.	Max.	Definition
t_C	10 µs	-	Reset pulse width.

3.3   Parallel Interface Operation

3.3.1   General Description

The parallel interface is based on an internal memory architecture, that allows the Anybus
CompactCom module to be interfaced directly as a memory mapped peripheral. The M40
modules can be configured for 8-bit or 16-bit parallel operation. The access time is 30 ns.

Polled operation is possible, but at the cost of an overhead. For increased efficiency, an optional
interrupt request signal (IRQ) can relieve the host application from polling for new information,
thus increasing the performance.

The parallel interface must be enabled using OM[0...3].

3.3.2   Pin Usage in 8-bit Parallel Mode

The parallel 8-bit interface uses the following signals:

Pin	Signal Name	Pin Type	Description/Comments
4 5 6 7 9 10 11 12 13 15 16 17 19 20	A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13	I	A[0...3]: Mandatory address input signals.
31 29 27 26 25 23 22 21	D0 D1 D2 D3 D4 D5 D6 D7	I/O	Standard bidirectional data bus.
49 48 47 46 45 43 42 41	LED1B LED1A LED2B LED2A $\overline{\text{LED3B}}$ $\overline{\text{LED3A}}$ $\overline{\text{LED4B}}$ $\overline{\text{LED4A}}$	O O O O OD OD O O	8-bit mode: LED functionality, see *LED Interface, p. 9*.
37	$\overline{\text{WE}}$	I	Active low write signal or combined read/write signal.
39	$\overline{\text{OE}}$	I	Bus output enable; enables output on the data bus when low.
36	$\overline{\text{CS}}$	I	Bus chip select enable; enables parallel access to the module when low.
38	$\overline{\text{IRQ}}$	O	Active low Interrupt Request signal. Asserted by the Anybus CompactCom module. The use of this signal is optional but highly recommended. Even if the host application lacks interrupt capabilities, it is recommended to connect this signal to an input port to simplify software design. This signal must be pulled to 3V3 on the host application side to prevent spurious interrupts during startup.
32 33 35	OM0 OM1 OM2	I	Operating mode. Connect all three to GND for 8-bit parallel operating mode. For more information see *Operating Modes, p. 16*.

Pin	Signal Name	Pin Type	Description/Comments
52	OM3 / ASI TX	O, I	Black channel output. See *Black Channel/Safety Interface, p. 51*. During startup the pin (with OM[0..2]) is used to define the operating mode of the module. Connect to external pull-up for 8-bit parallel operating mode, see *Pin Overview, p. 12*.
51	ASI RX	I	Black channel input. Tie to 3V3 if not used. See *Black Channel/Safety Interface, p. 51*
54 53	MI0/SYNC MI1	O	See *Module Identification, p. 16*
30	MD0	O	See *Module Detection, p. 16*
3	$\overline{RESET}$	I	See *RESET (Reset Input), p. 18*.

ℹ️ *There are no internal pull-up resistors on any of the signals above, except for OM3, which has an internal weak pull-up.*

Function Table (CS, WE, OE, D[0...7])

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	D[0...7] State	Comment
HIGH	X	X	High impedance	Module not selected.
LOW	LOW	X	Data Input (Write)	Data on D[0...7] is written to location selected by address bus.
LOW	HIGH	LOW	Data Output (Read)	Data from location selected by address bus is available on D[0...7].
LOW	HIGH	HIGH	High impedance	Module is selected, but D[0...7] is in a high impedance state.

X = don't care

LOW = V_{IL}

HIGH = V_{IH}

3.3.3 Pin Usage in 16-bit Parallel Mode

The parallel 16-bit interface uses the following signals:

Pin	Signal Name	Pin Type	Description/Comments
5 6 7 9 10 11 12 13 15 16 17 19 20	A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13	I	A[1...13]: Mandatory address input signals. Selects source/target location.
31 29 27 26 25 23 22 21 49 48 47 46 45 43 42 41	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	I/O	Standard bidirectional data bus.
4	$\overline{\text{WEH}}$	I	Write enable high byte.
37	$\overline{\text{WEL}}$	I	Write enable low byte.
39	$\overline{\text{OE}}$	I	Bus output enable; enables output on the data bus when low.
36	$\overline{\text{CS}}$	I	Bus chip select enable; enables parallel access to the module when low.
38	$\overline{\text{IRQ}}$	O	Active low Interrupt Request signal. Asserted by the Anybus CompactCom module. The use of this signal is optional but highly recommended. Even if the host application lacks interrupt capabilities, it is recommended to connect this signal to an input port to simplify software design. This signal must be pulled to 3V3 on the host application side to prevent spurious interrupts during startup.
32 33 35	OM0 OM1 OM2	I	Operating mode. Connect all three to 3V3 for 16-bit parallel operating mode. For more information see *Operating Modes, p. 16*
54 53	MI0/SYNC MI1	O	See *Module Identification, p. 16*
52	OM3 / ASI TX	O, Strap	Black channel output. See *Black Channel/Safety Interface, p. 51* During startup the pin (with OM[0..2]) is used to define the operating mode of the module. Connect to pull-down for 16-bit parallel operating mode, see *Pin Overview, p. 12*.
51	ASI RX	I	Black channel input. Connect to 3V3 if not used. See *Black Channel/Safety Interface, p. 51*
30	MD0	O	See *Module Detection, p. 16*.
3	$\overline{\text{RESET}}$	I	See *RESET (Reset Input), p. 18*

The A0 signal is not needed in 16-bit parallel operating mode, as 16 bits are addressed instead of 8 bits. If there is need for writing one byte at the time signals $\overline{\text{WEH}}$ and $\overline{\text{WEL}}$ can be used to enable writing to the high or low byte respectively. If both are enabled both bytes are written.

Function Table (CS, WEL, WEH, OE, D[0...15])

$\overline{\text{CS}}$	$\overline{\text{WEL}}$	$\overline{\text{WEH}}$	$\overline{\text{OE}}$	D[0...15] State	Comment
HIGH	X	X	X	High impedance	Module not selected.
LOW	LOW	HIGH	X	Data Input (Write)	Data on D[0...7] is written to low byte of location selected by address bus.
LOW	HIGH	LOW	X	Data Input (Write)	Data on D[8...15] is written to high byte of location selected by address bus.
LOW	LOW	LOW	X	Data Input (Write)	Data on D[0 ...15] is written to location selected by address bus.
LOW	HIGH	HIGH	LOW	Data Output (Read)	Data from location selected by address bus is available on D[0...15].
LOW	HIGH	HIGH	HIGH	High impedance	Module is selected, but D[0...15] is in a high impedance state.

X = don't care

LOW = V_{IL}

HIGH = V_{IH}

3.3.4 Memory Access Read Timing

The $\overline{WE}$ input signal must remain high during a read access. The timing diagram shows a burst read, but the timing applies for a single read as well. The Anybus CompactCom B40-1 has no setup or hold timing requirements on the address bus relative to $\overline{CS}$ during read operations. The only limitation on read setup and hold times is that the pingpong and powerup interrupt will be acknowledged if all address lines are high for 10-15 ns or more while $\overline{CS}$ is low.
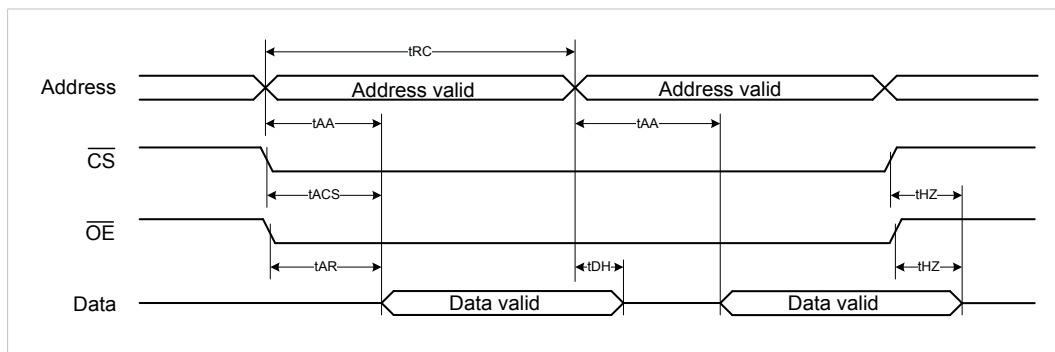
Fig. 7

Symbol	Parameter	Min (ns)	Max (ns)
tRC	Read cycle time	30	-
tAA	Address valid to Data valid	-	30
tACS	$\overline{CS}$ low to Data valid	-	30
tAR	**OE** low to Data valid	-	15
tHZ	$\overline{CS}$ or $\overline{OE}$ high to output reached tristate	-	15
tDH	Data hold time	0	-

3.3.5 Memory Access Write Timing

It doesn't matter if the $\overline{OE}$ signal is low or high as long as $\overline{WE}$ is active (low). In 16 bit mode, the timing requirements of $\overline{WE}$ applies to both $\overline{WEL}$ and $\overline{WEH}$. The timing diagrams show a burst write but the timing applies for a single write as well. The first diagram shows write enable controlled write timing and the second shows chip select controlled write timing.
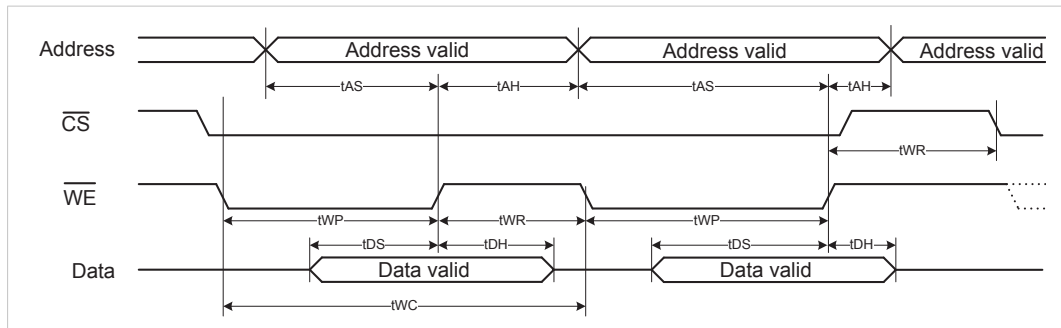
Fig. 8
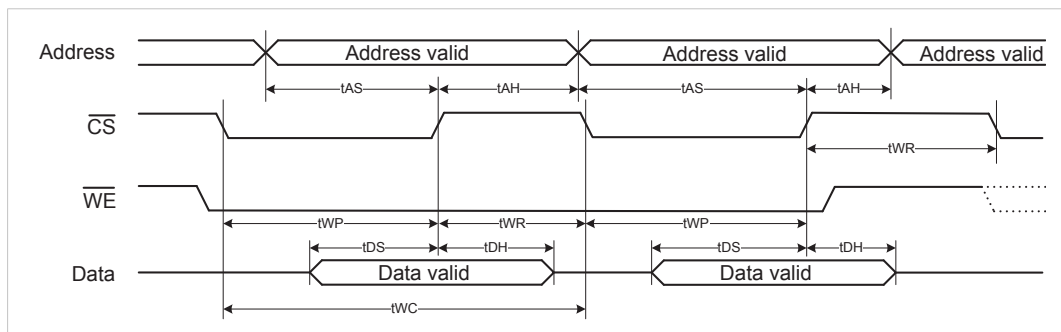
Fig. 9

Symbol	Parameter	Min (ns)	Max (ns)
tWC	Write cycle time	30	-
tAS	Address valid before End-of-Write	15	-
tAH	Address valid after End-of-Write	0	-
tWP	$\overline{CS}$ and $\overline{WE}$ low pulse width	15	-
tDS	Data valid before End-of-Write	15	-
tDH	Data valid after End-of-Write	0	-
tWR	Write recovery time	10	-

3.4   SPI Operation

3.4.1   General Description

The SPI (Serial Peripheral Interface) bus is a synchronous serial data link standard which operates in full duplex mode.

The SPI interface is activated using the OM[0...3] inputs. See *Operating Modes, p. 16*.

3.4.2   Pin Usage in SPI Mode

Presented below is an overview of all pins except GND and 3V3.

Pin	Signal Name	Type	Description/Comments
4 5 6 7 9 10 11 12	DIP1_0 DIP1_1 DIP1_2 DIP1_3 DIP1_4 DIP1_5 DIP1_6 DIP1_7	I I I I I I I I	DIP switch. Usage defined by application. Readable through attribute #14 (Switch status) in Anybus Object, instance #1. Tie to GND if not used.
13	$\overline{\text{SS}}$	I	Slave select. Active low.
15	SCLK	I	Serial Clock Input
16	MISO	O	Master input, slave output. Input to the master's shift register, and output from the slave's shift register.
17	MOSI	I	Master output, slave input. Output from the master's shift register, and input to the slave's shift register.
19 20	(not used)	I O, I	Tie to 3V3.
31 29 27 26 25 23 22 21	DIP2_0 DIP2_1 DIP2_2 DIP2_3 DIP2_4 DIP2_5 DIP2_6 DIP2_7	I I I I I I I I	DIP switch. Usage defined by application. Readable through attribute #14 (Switch status) in Anybus Object, instance #1. Tie to GND if not used.
49 48 47 46 45 43 42 41	LED1B LED1A LED2B LED2A $\overline{\text{LED3B}}$ $\overline{\text{LED3A}}$ $\overline{\text{LED4B}}$ $\overline{\text{LED4A}}$	O O O O OD OD O O	LED interface. Gives access to LED indications. For more information, see *LED Interface / D8–D15 (Data Bus), p. 14*".
37 39 36	(not used)	I	Tie to 3V3.
38	$\overline{\text{IRQ}}$	O	Active low Interrupt Request signal. Asserted by the Anybus CompactCom module. The use of this signal is optional but highly recommended. Even if the host application lacks interrupt capabilities, it is recommended to connect this signal to an input port to improve the startup time. This signal must be pulled to 3V3 on the host application side to prevent spurious interrupts during startup.
32 33 35	OM0 OM1 OM2	I	Operating mode [OM2, OM1, OM0]: 0,0,1 for SPI operating mode. For more information see *Operating Modes, p. 16*
52	OM3 / ASI TX	O, Strap	Black channel output. See *Black Channel/Safety Interface, p. 51* During startup the pin (with OM[0..2]) is used to define the operating mode of the module. Connect to external pull-down for SPI operating mode,see *Pin Overview, p. 12*.

Pin	Signal Name	Type	Description/Comments
51	ASI RX	I	Black channel input. Connect to 3V3 if not used. See *Black Channel/Safety Interface, p. 51*
54 53	MI0/SYNC MI1	O	See *Module Identification, p. 16*
30	MD	O	See *Module Detection, p. 16*
3	$\overline{\text{RESET}}$	I	See *RESET (Reset Input), p. 18*

3.4.3 SPI Interface Signals

The SPI interface option uses three (optionally four) signals:

Signal	Description
SCLK	Serial Clock Input
MOSI	Master output, slave input. Output from the master's shift register, and input to the slave's shift register.
MISO	Master input, slave output. Input to the master's shift register, and output from the slave's shift register.
$\overline{\text{SS}}$	Slave Select (optional)

For increased efficiency, the interrupt request signal ($\overline{\text{IRQ}}$) is also available, allowing the host application to service the Anybus CompactCom module only when necessary.

4–Wire Mode

In 4-wire mode the $\overline{SS}$ signal is used to indicate the start and stop of an SPI transfer. In this mode the SCLK signal is allowed to be either idle high or idle low. This mode also allows multiple SPI slaves on the same SPI bus, since Anybus CompactCom MISO is tri-stated when $\overline{SS}$ is high.

A 4-wire diagram example:
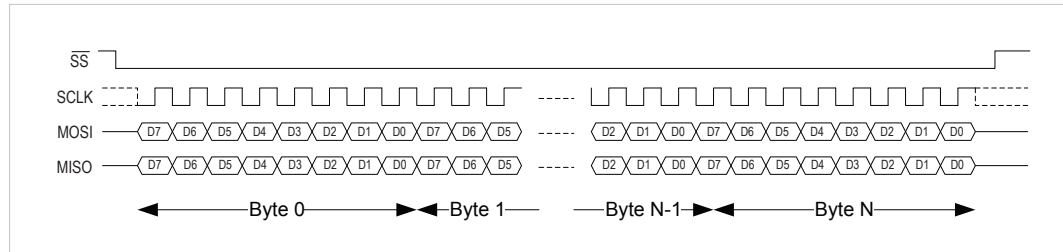
Fig. 10

Fig. 11

Item	Description	Min Value	Max Value
tSU	MOSI setup before SCK rising edge	10 ns	-
tHD	MOSI hold after SCK rising edge	10 ns	-
tDO	MISO change after SCK falling edge	0 ns	20 ns
tCL	SCK low period	20 ns	-
tCH	SCK high period	20 ns	-
tCL+tCH	SCK period. Max. frequency supported is 20 MHz.	50 ns	-
tCSS	$\overline{SS}$ setup before first SCLK rising edge.	20ns	-
tCSH	$\overline{SS}$ hold after last SCLK rising edge.	20ns	-
tCSLZ	MISO valid after falling edge of $\overline{SS}$.	-	20ns
tCSHZ	MISO high-Z after rising edge of $\overline{SS}$.	-	20ns

3–Wire Mode

In 3-wire mode the $\overline{SS}$ signal must be tied low permanently, and the SCLK signal must be idle high. Multiple SPI slaves on the same bus are not possible in this mode. The module detects start and stop of a transfer by monitoring SCLK activity.

There must be an idle period of at least 10 μs between two transfers in this mode, and the SCLK signal must never remain high for more than 5 μs during a transfer.

A 3-wire diagram example.
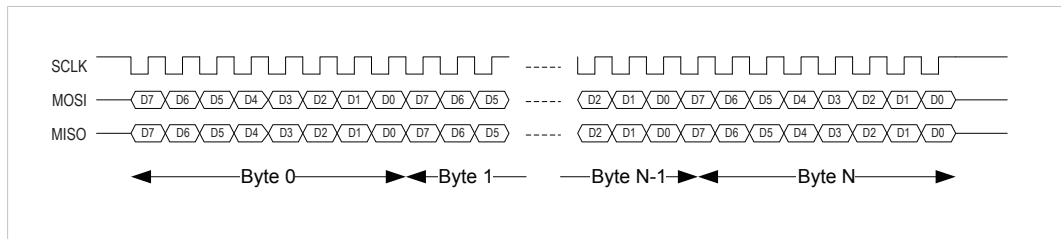
Fig. 12

SPI diagram and bit timing for 3-wire mode.

Fig. 13

Item	Description	Min Value	Max Value
tSU	MOSI setup before SCK rising edge	10 ns	-
tHD	MOSI hold after SCK rising edge	10 ns	-
tDO	MISO change after SCK falling edge	0 ns	20 ns
tCL	SCK low period	20 ns	-
tCH	SCK high period	20 ns	-
tCL+tCH	SCK period Max. frequency supported is 20 MHz.	50 ns	-

SPI Frame Format
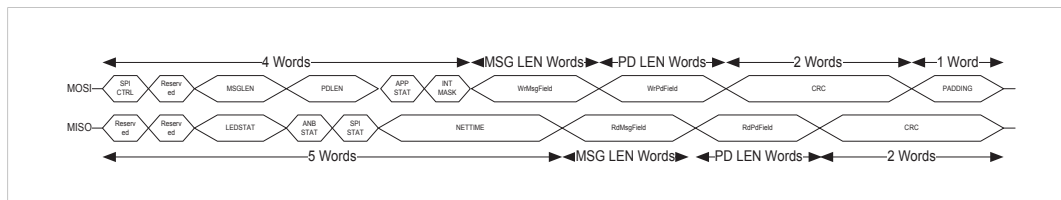
Fig. 14

The bytes are transmitted with the most significant bit first. The byte order for non-byte frame elements is typically little endian. This means that the least significant byte is transmitted first. The CRC32 checksum is an exception as it is transmitted in big endian byte order (most significant byte first).

3.5   Stand-alone Shift Register

3.5.1   General Information

In this mode the Anybus CompactCom B40-1 operates stand-alone, with no host processor. Process data is communicated to shift registers on the host. The Anybus CompactCom B40-1 supports up to 32 registers in each direction, for a total of 256 bits of data.
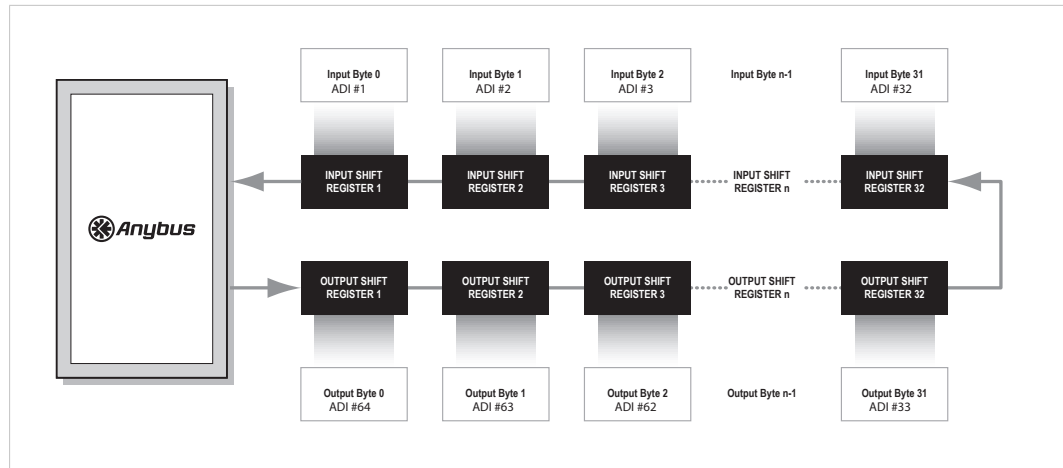
Fig. 15

Even though the Anybus CompactCom B40-1 operates stand-alone, it is still possible to set host application attributes, via the use of the virtual attributes list. Some attributes are mandatory to implement in order to pass conformance test. See the Virtual Attributes section in the Anybus CompactCom 40 Software Design Guide for more information.

The Anybus CompactCom B40-1 will automatically detect the number of connected input and output shift registers. Every shift register will be represented by one UINT8 ADI. The input ADIs will be named "Input 0", "Input 1", etc. The output ADIs will be named "Output 0", "Output 1", etc.

> ⓘ *The ADI access descriptor values cannot be changed:*
>
> *Input ADIs: 09h (Get access + Write process data mapping possible).*
>
> *Output ADIs: 11h (Get access + Read process data mapping possible)*

Bits are clocked out/in MSB first, on the positive side of CLK. An active low load signal ($\overline{LD}$) loads all shift registers before and after a transfer.
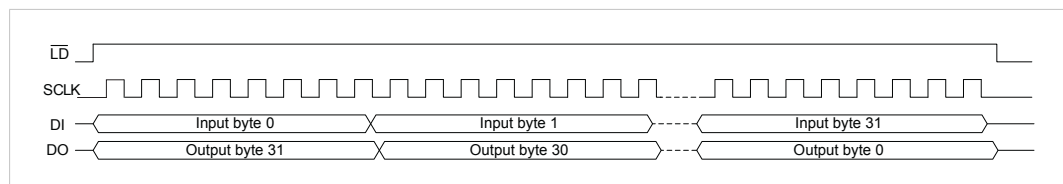
Fig. 16

A fifth signal, PA, is high when the module is in active state, and low when the module is not. This signal can be used by the application to clear/set the output shift registers to default values when the module is not in active state.

3.5.2   Pin Usage in Stand-Alone Shift Register Mode

Presented below is an overview of all pins except GND and V_{DD}.

Pin	Signal Name	Type	Description/Comments
4 5 6 7 9 10 11 12	DIP1_0 DIP1_1 DIP1_2 DIP1_3 DIP1_4 DIP1_5 DIP1_6 DIP1_7	I I I I I I I I	DIP switch node address / IP address. See *DIP1 and DIP2 Pins Usage, p. 32*.
13	$\overline{LD}$	O	Shift register load.
15	SCLK	O	Clock output.
16	DO	O	Serial data output to shift registers.
17	DI	I	Serial data input from shift registers.
19	(not used)	-	Leave unconnected
20	(not used)	-	Leave unconnected
31 29 27 26 25 23 22 21	DIP2_0 DIP2_1 DIP2_2 DIP2_3 DIP2_4 DIP2_5 DIP2_6 DIP2_7	I I I I I I I I	DIP switch baud rate / Device ID / station name. See *DIP1 and DIP2 Pins Usage, p. 32*.
49 48 47 46 45 43 42 41	LED1B LED1A LED2B LED2A $\overline{LED3B}$ $\overline{LED3A}$ $\overline{LED4B}$ $\overline{LED4A}$	O O O O OD OD O O	LED interface. Gives access to LED indications. For more information, see *LED Interface / D8–D15 (Data Bus), p. 14*.
37	CT	I	Center tap signal for shift register mode. The number of connected input and output shift registers will be detected using this signal.
38	PA	O	Process active signal for shift register mode. In a PROFINET shift register stand-alone application, the PA signal must be used to clear outputs, when the Anybus CompactCom B40-1 is not in state PROCESS ACTIVE. Otherwise it will not be possible to certify the final product. See the Anybus CompactCom 40 PROFINET IRT Network Guide for more information.
39	(not used)	-	Leave unconnected.
36	(not used)	-	Leave unconnected.
51	ASI RX	I	Black channel input. Connect to 3V3 if not used. See *Black Channel/Safety Interface, p. 51*
52	ASI TX / OM3	O, Strap	Black channel output. See *Black Channel/Safety Interface, p. 51* During startup the pin (with OM[0..2]) is used to define the operating mode of the module. Connect to external pull-down for shift register operating mode, see *Pin Overview, p. 12*.
32 33 35	OM0 OM1 OM2	I	Operating mode [OM2, OM1, OM0]: 0,1,0 for shift register operating mode. For more information see*Operating Modes, p. 16*.
54 53	MI0/SYNC MI1	O	See *Module Identification, p. 16*.
30	MD	O	See *Module Detection, p. 16*.
3	$\overline{RESET}$	I	See*RESET (Reset Input), p. 18*

DIP1 and DIP2 Pins Usage

The use of the DIP1 and DIP2 pins is network specific. If used, they will be read during SETUP state. Thereafter, DIP switch changes will be sampled and written to the Network Configuration Object every 0.5 seconds.

DIP1 is linked to the Network Configuration Object, instance 1 (node address) or instance 3 (IP address). DIP2 is linked to the Network Configuration Object, instance 2 (baud rate) or instance 1 (Device ID, EtherCAT), or, in the case of PROFINET, linked to the PROFINET IO Object , instance 1, attribute 24.

See Network Configuration Object (04h) in the Anybus CompactCom 40 Software Design Guide for more information.

Network	DIP1 (linked to Network Configuration Object)	DIP2	Notes
DeviceNet	0 - 63 (Instance 1: Node address)	Value: 0 - 3 (Network Configuration Object, Instance 2: Baud Rate)	DIP2: Network Configuration Object, Instance 2: Baud Rate (125 kbps, 250 kbps, 500 kbps, Auto)
EtherCAT	1 - 254 (Instance 3: IP address)	0 - 255 (Network Configuration Object, Instance 1: Device ID)	If DIP1 is set to 0, saved values from instances 3 - 6 are used. If DIP1 is set to 255, DHCP is used for all settings. The DIP switches set the last byte of the IP address. Virtual attributes are used to configure the remaining part of the IP address, as well as the subnetmask (Network Configuration Object, instance 4) and the gateway (instance 5).
EtherNet/IP	1 - 254 (Instance 3: IP address)	Not used	
Modbus-TCP	1 - 254 (Instance 3: IP address)	Not used	
Common Ethernet	1 - 254 (Instance 3: IP address)	Not used	
Ethernet POWERLINK	NMT_CS_BASIC_ETHERNET: 1 - 254 (Instance 3: IP address) NMT_CS_EPL_MODE: 1 - 239 (Instance 1: Node address)	Not used	If no POWERLINK traffic is seen at startup the module will enter the NMT_CS_BASIC_ETHERNET state after 5 seconds. In this state DIP1 is used for the IP address. As soon as the module detects POWERLINK traffic it will enter the NMT_CS_EPL_MODE super state. In this state DIP1 is used as the POWERLINK node address. In the NMT_CS_EPL_MODE state the IP address of the module is fixed to 192.168.100.yyy where yyy is the node address. Note that IT functionality can be disabled in the POWERLINK host application object. If that is done DIP1 is never used for the IP address.
PROFIBUS	0 - 126 (Instance 1: Node address)	Not used	-

Network	DIP1 (linked to Network Configuration Object)	DIP2	Notes
PROFINET	1 - 254 (Instance 3: IP address)	Value: 1 — 255 (PROFINET IO object, Instance 1, attribute 24)	If DIP1 is set to 0, saved values from instances 3 - 6 are used. If DIP1 is set to 255, DHCP is used for all settings. The DIP1 to switches set the last byte of the IP address. Virtual attributes are used to configure the remaining part the IP address, as well as the subnetmask (Network Configuration Object, instance 4) and the gateway (instance 5). If DIP2 is set to 0, the value saved in the non volatile memory will be used. The DIP2 switches set the last three digits of the station name. see the Anybus CompactCom 40 PROFINET IRT Network Guide.
CC-Link	1 - 64 (Instance 1: Node address).	Value: 0 - 4 (Network Configuration Object, Instance 2: Baud Rate)	DIP1: Depending on number of stations used. An invalid value will generate a NACK on Setup Complete. DIP2: Network Configuration Object, Instance 2: Baud Rate (156 kbps, 625 kbps, 2.5 Mbps, 5 Mbps, 10 Mbps)
CC-Link IE Field	1 - 120 (Instance 1: Station Number).	1 - 239 (Instance 3: Network Number).	-
BACnet/IP	1 - 254 (Instance 3: IP address)	Not used	-
CANopen	0 - 127 (Instance 1: Node address)	Value: 0 - 9 (Network Configuration Object, Instance 2: Data Rate)	DIP2: Network Configuration Object, Instance 2: Data Rate

Unused DIP pins should be connected to ground (GND).

External pull-down resistors are needed if DIP switches are connected to the DIP1 and DIP2 pins, see .

3.5.3   Timing

The Anybus CompactCom B40-1 operates in 12.5 MHz in shift register mode.

Timing Diagram
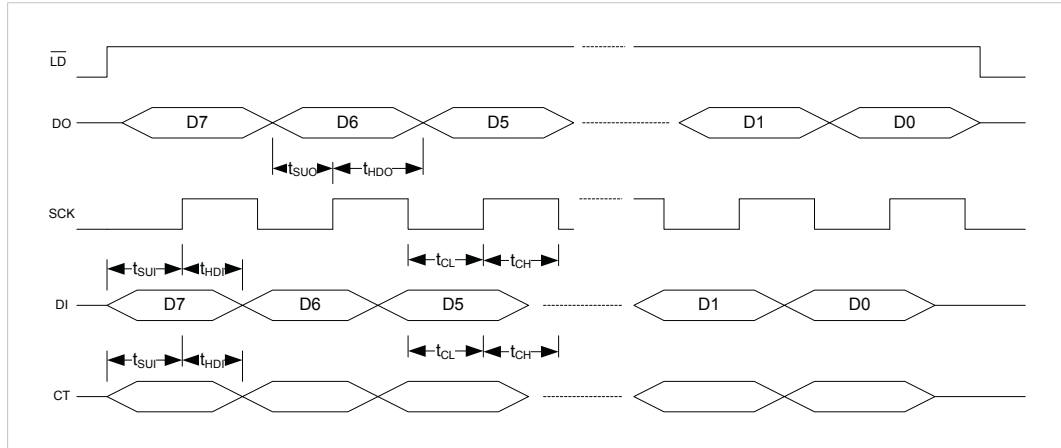
Fig. 17

Abbreviations from the diagram above, explained, and timing details:

Item	Description	Min Value
tSUO	DO setup before SCK rising edge	20 ns
tHDO	DO hold after SCK rising edge	20 ns
tSUI	DI/CT setup before SCK rising edge	10 ns
tHDI	DI/CT hold after SCK rising edge	0 ns
tCH	SCK high period	35 ns
tCL	SCK low period	35 ns
tCH + tCL	SCK period	78 ns

The idle time between two transfers, i.e. when the $\overline{LD}$ signal is low, is at least 1 μs.

The cycle time range is typically 160 μs to 200 μs. However it is highly module and network dependent, and may differ from the defined range.

3.5.4   Basic Shift Register Circuit

The schematic below illustrates a basic shift register circuit.
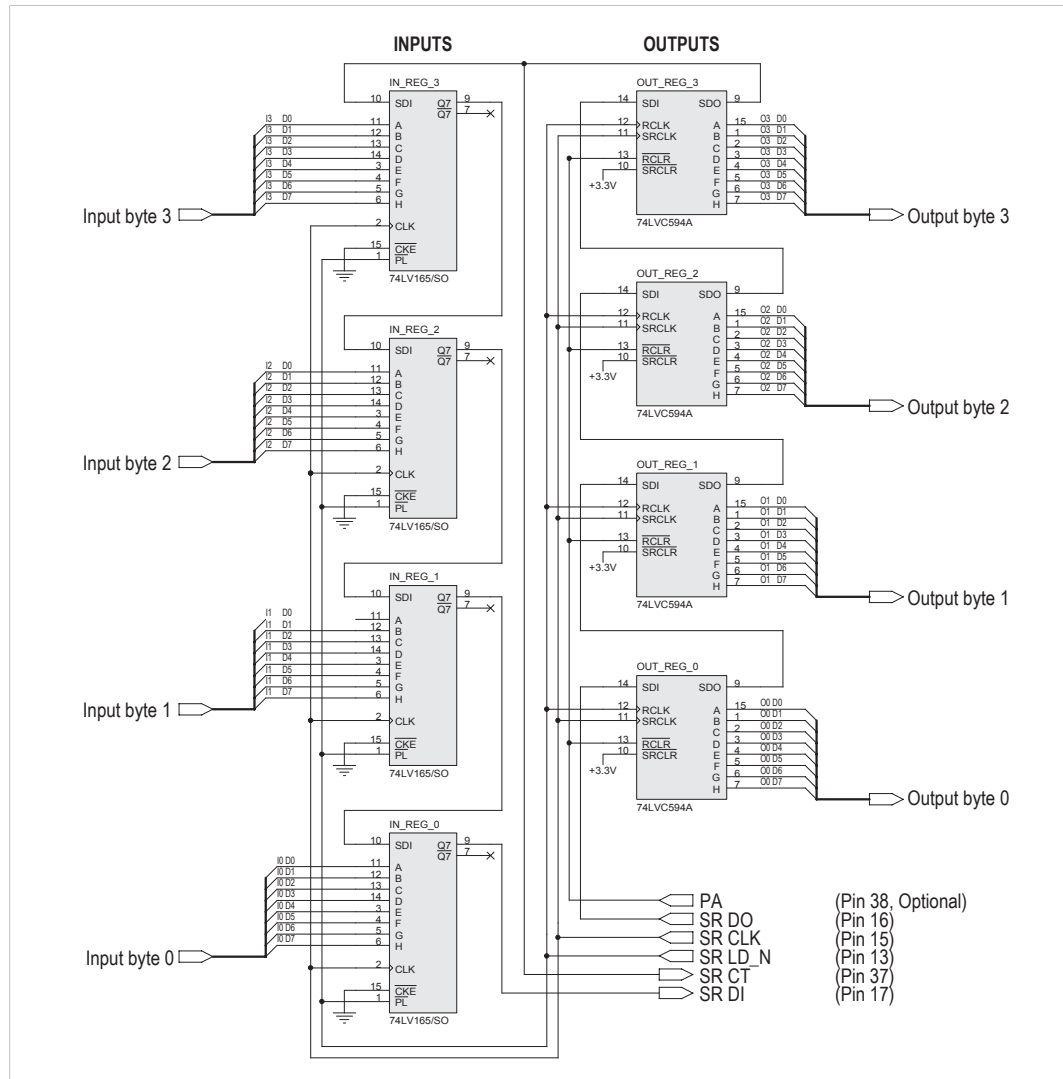
Fig. 18

3.5.5 Reset Circuit Example

The reset circuit example in the figure, is a common 3.3 V supervisor. The main usage is to obtain a defined reset release delay after the voltage is switched on. The power supply has to provide a stable voltage within the interval 3.15–3.45 V
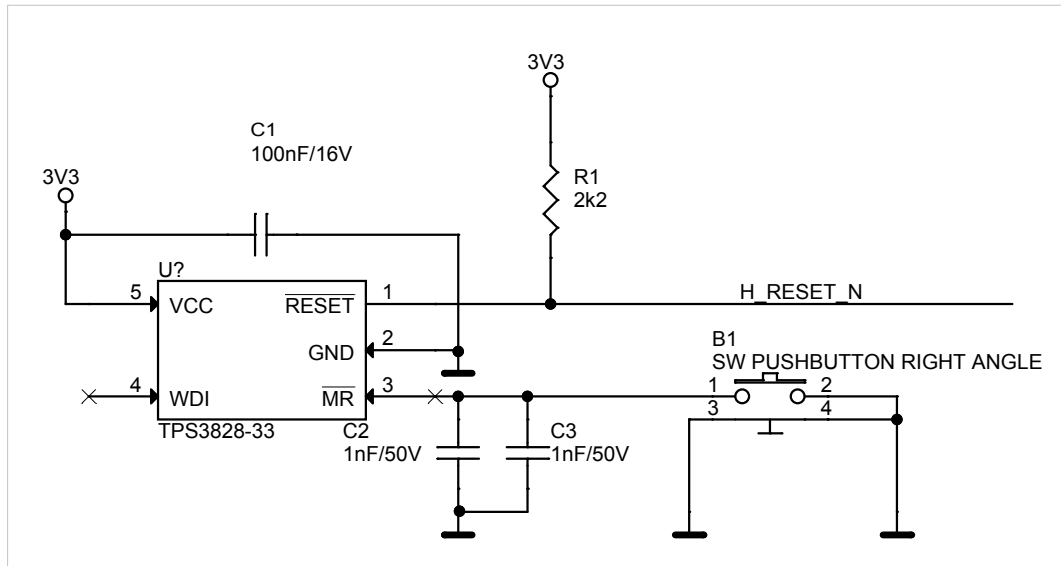
Fig. 19

3.5.6 DIP Switches Example

Pull-down resistors are necessary if DIP switches are connected to the DIP inputs.
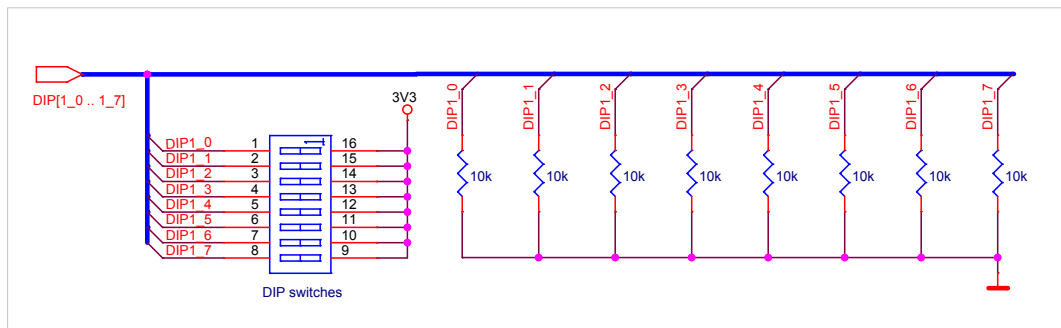
Fig. 20

3.6   UART Operation

3.6.1   General Description

The serial interface is a common asynchronous serial interface, which can easily be interfaced directly to a microcontroller or UART. It is provided for backward compatibility with the Anybus CompactCom 30 series.

The serial interface is activated using the OM[0...3] inputs, which also are used to select the operating baud rate, see *Operating Modes, p. 16*.

Other communication settings are fixed to the following values:

Data bits: 8

Parity: None

Stop bits: 1

Communication settings are fixed to asynchronous, 8-N-1, with bit order LSB first and without hardware flow control signals.

$(\mathbf{i})$ *It is not possible to build a synchronous application in this mode.*

3.6.2   Pin Usage in Serial Mode

Presented below is an overview of all pins except GND and 3V3

Pin	Signal Name	Pin Type	Description/Comments
4 5 6 7 9 10 11 12	DIP1_0 DIP1_1 DIP1_2 DIP1_3 DIP1_4 DIP1_5 DIP1_6 DIP1_7	I I I I I I I I	DIP switch. Usage defined by application. Readable through attribute #14 (Switch status) in Anybus Object, instance #1. Connect directly to GND if not used.
13 15 16	(not used)	I I O,I	Connect directly to GND
17	(not used)	I	Connect directly to 3V3.
19	ASI RX	I	See *Black Channel/Safety Interface, p. 51* If not used, connect directly to 3V3.
20	ASI TX	O	See *Black Channel/Safety Interface, p. 51* If not used, leave unconnected.
31 29 27 26 25 23 22 21	DIP2_0 DIP2_1 DIP2_2 DIP2_3 DIP2_4 DIP2_5 DIP2_6 DIP2_7	I I I I I I I I	DIP switch. Usage defined by application. Readable through attribute #14 (Switch status) in Anybus Object, instance #1. Connect directly to GND if not used.
49 48 47 46 45 43 42 41	LED1B LED1A LED2B LED2A LED3B $\overline{\text{LED3A}}$ $\overline{\text{LED4B}}$ $\overline{\text{LED4A}}$	O O O O OD OD O O	LED interface. Gives access to LED indications. For more information, *LED Interface / D8–D15 (Data Bus), p. 14*. When not used, LED1A, LED1B, LED2A, LED2B, LED4A and LED4B can be left unconnected. LED3A and LED3B are open-drain outputs and should, if not used, be pulled either to GND or to 3V3, depending on application.
37 39 36	(not used)	I I I	Connect directly to 3V3.
38	(not used)	O	Leave unconnected
51	RX	I	Receive Input • Direction: Host application -> CompactCom • Idle state = High

Pin	Signal Name	Pin Type	Description/Comments
52	TX / OM3	O, I	Transmit Output • Direction: CompactCom -> Host application • Idle state = High This pin doubles as OM3 strapping input on Anybus CompactCom M40 modules. Connect a pull-up resistor on the application for this pin in serial mode.
32 33 35	OM0 OM1 OM2	I	Operating mode [OM2, OM1, OM0]: | 001	Serial 19.2 kbps
010	Serial 57.6 kbps
011	Serial 115.2 kbps
100	Serial 625 kbps	 For more information see *Operating Modes, p. 16*.
54 53	MI0/SYNC MI1	O	See *Module Identification, p. 16*
30	MD0	O	See *Module Detection, p. 16*
3	$\overline{\text{RESET}}$	I	See *RESET (Reset Input), p. 18*

ⓘ   *It is important to connect all signals correctly for proper functioning of the serial interface.*

3.6.3   Baud Rate Accuracy

As with most asynchronous communication devices, the actual baud rate used on the Anybus CompactCom may differ slightly from the ideal baud rate.

The baud rate error of the module is less than ±1.5%. For proper operation, it is recommended that the baud rate accuracy in the host application lies within ±1.5% from the ideal value.

4 Network Connector

The network connector provides network access to the brick.
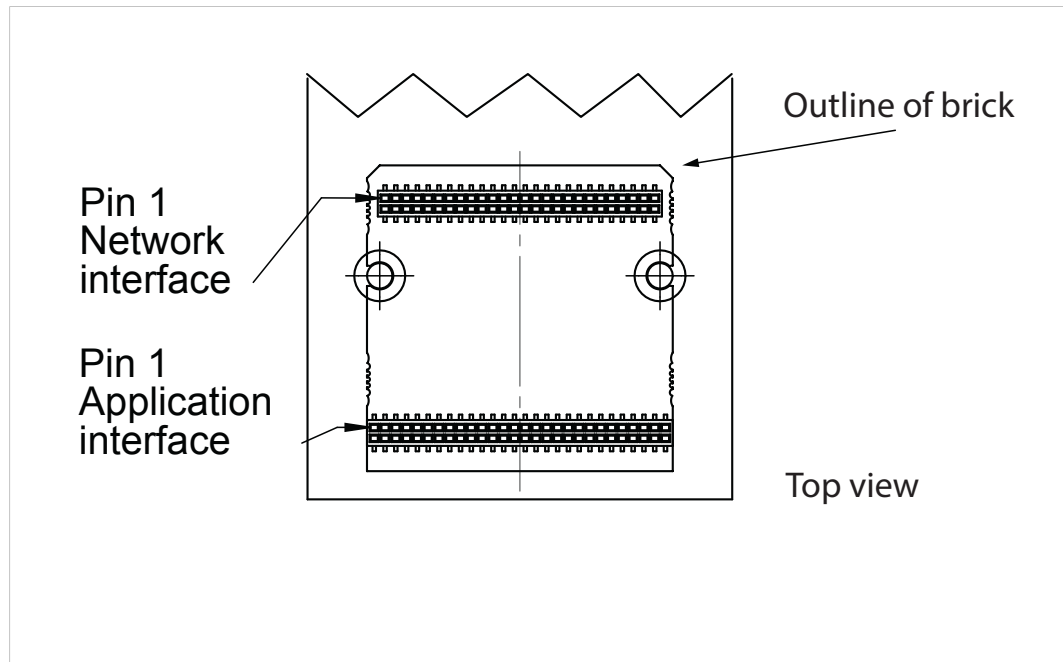
Fig. 21

The signals from the brick network connector can be directly routed to the (optional) connector board, which carries a network connector(s) identical or similar to the ones on the corresponding Anybus CompactCom M40 module.

Examples on how to design the network access circuitry, when not using the connector board, are shown in *Design Examples, Network Interface, p. 74*.

The brick has a standard 1.27 mm 52 pin header surface mounted to the bottom side of the board as network interface.
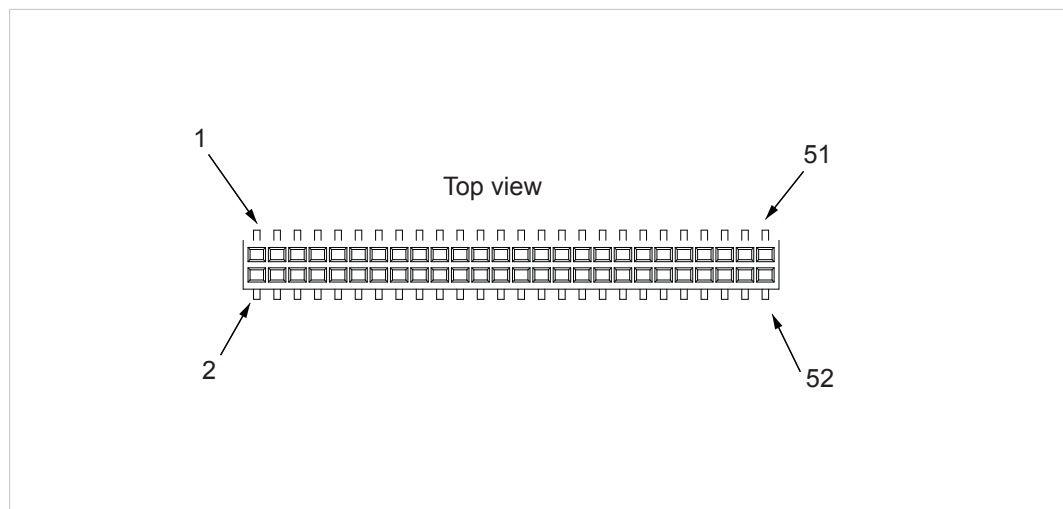
Fig. 22

The pictures shows the pinning of the corresponding network connector on the host application board, seen from the top.

```
                    GND   2  ☐  ☐  1   3V3
              B_1CEN/SDA   4  ☐  ☐  3   B_1P/RXP
                    GND   6  ☐  ☐  5   B_1N/RXN
              B_2CEN/SCL   8  ☐  ☐  7   B_2P/SDP
                    GND  10  ☐  ☐  9   B_2N/SDN
                 B_3CEN  12  ☐  ☐  11  B_3P/TXEN
                    GND  14  ☐  ☐  13  B_3N/TXDIS
             B_4CEN/BUSP  16  ☐  ☐  15  B_4P/TXP
                    GND  18  ☐  ☐  17  B_4N/TXN
               NW_LED4A  20  ☐  ☐  19  NW_LED4B
               NW_LED3A  22  ☐  ☐  21  NW_LED3B
               NW_LED2A  24  ☐  ☐  23  NW_LED2B
               NW_LED1A  26  ☐  ☐  25  NW_LED1B
                    GND  28  ☐  ☐  27  3V3
              A_1CEN/SDA  30  ☐  ☐  29  A_1P/RXP
                    GND  32  ☐  ☐  31  A_1N/RXN
              A_2CEN/SCL  34  ☐  ☐  33  A_2P/SDP
                    GND  36  ☐  ☐  35  A_2N/SDN
                 A_3CEN  38  ☐  ☐  37  A_3P/TXEN
                    GND  40  ☐  ☐  39  A_3N/TXDIS
             A_4CEN/BUSP  42  ☐  ☐  41  A_4P/TXP
                    GND  44  ☐  ☐  43  A_4N/TXN
                   C_RX  46  ☐  ☐  45  C_TX
                 C_BUSP  48  ☐  ☐  47  C_TXEN
                  GATE2  50  ☐  ☐  49  GATE1
                    GND  52  ☐  ☐  51  3V3
```

Fig. 23

4.1   Overview

Depending on network, the pins have different names and different functionality. Presented below is an overview of all pins except GND and 3V3. More detailed descriptions of the signals are described for each network/fieldbus version later in this section (*4*).

Pin	Signal Name				
	Ethernet based networks, Copper	Ethernet based networks, fiber optic	DeviceNet	PROFIBUS	CC-Link
3	B_1P	B_RXP			
4	B_1CEN	B_SDA			
5	B_1N	B_RXN			
7	B_2P	B_SDP			
8	B_2CEN	B_SCL			
9	B_2N	B_SDN			
11	B_3P	B_TXEN			
12	B_3CEN				
13	B_3N	B_XDIS			
15	B_4P	B_TXP			
16	B_4CEN				
17	B_4N	B_TXN			
19	NW_LED4B	NW_LED4B	NW_LED4B	NW_LED4B	NW_LED4B
20	NW_LED4A	NW_LED4A	NW_LED4A	NW_LED4A	NW_LED4A
21	NW_LED3B	NW_LED3B	NW_LED3B	NW_LED3B	NW_LED3B
22	NW_LED3A	NW_LED3A	NW_LED3A	NW_LED3A	NW_LED3A
23	NW_LED2B	NW_LED2B	NW_LED2B	NW_LED2B	NW_LED2B
24	NW_LED2A	NW_LED2A	NW_LED2A	NW_LED2A	NW_LED2A
25	NW_LED1B	NW_LED1B	NW_LED1B	NW_LED1B	NW_LED1B
26	NW_LED1A	NW_LED1A	NW_LED1A	NW_LED1A	NW_LED1A
29	A_1P	A_RXP			
30	A_1CEN	A_SDA			
31	A_1N	A_RXN			
33	A_2P	A_SDP			
34	A_2CEN	A_SCL			
35	A_2N	A_SDN			
37	A_3P	A_TXEN			
38	A_3CEN				
39	A_3N	A_TXDIS			
41	A_4P	A_TXP			
42	A_4CEN				
43	A_4N	A_TXN			
45			C_TX	C_TX	C_TX
46			C_RX	C_RX	C_RX
47				C_TXEN	C_TXEN
48			C_BUSP_N		
49			GATE1	GATE1	GATE1
50			GATE2	GATE2	GATE2

At the moment the following copper wired Ethernet protocols are available: EtherNet/IP, PROFINET IRT, Ethernet POWERLINK, EtherCAT, Modbus-TCP, CC-Link IE Field and BACnet/IP. At the moment the following fiber optical Ethernet protocol is available: PROFINET IRT. The speed of all of these protocols are 100 Mb/s (using signal pairs 1-2 of each port), except CC-Link IE Field which is 1 Gb/s (using signal pairs 1–4 of each port).

The LED signals are active high and should be connected to respective LED via a resistor.

The pin types of the connector are defined in *PIN Types, p. 5*. The pin types are specified for each network type on the following pages.

4.2   Power Supply Pins

Signal Name	Type	Pin No.	Description
GND	Power	2, 6, 10, 14, 18, 28, 32, 36, 40, 44, 52	Ground Power and signal ground reference.
3V3	Power	1, 27, 51	3.3 V power supply.

4.3   How to Connect Unused Network Connector Pins

For Ethernet versions of the Anybus CompactCom B40-1 it is recommended to terminate Ethernet signals in the network interface if one of the Ethernet ports is unused. For the 10/100 Mb/s hardware version it is sufficient to terminate pair no. 1 and 2, for the port of concern, while for the 1 Gb/s hardware version this has to be done for pair no. 1, 2, 3, and 4.
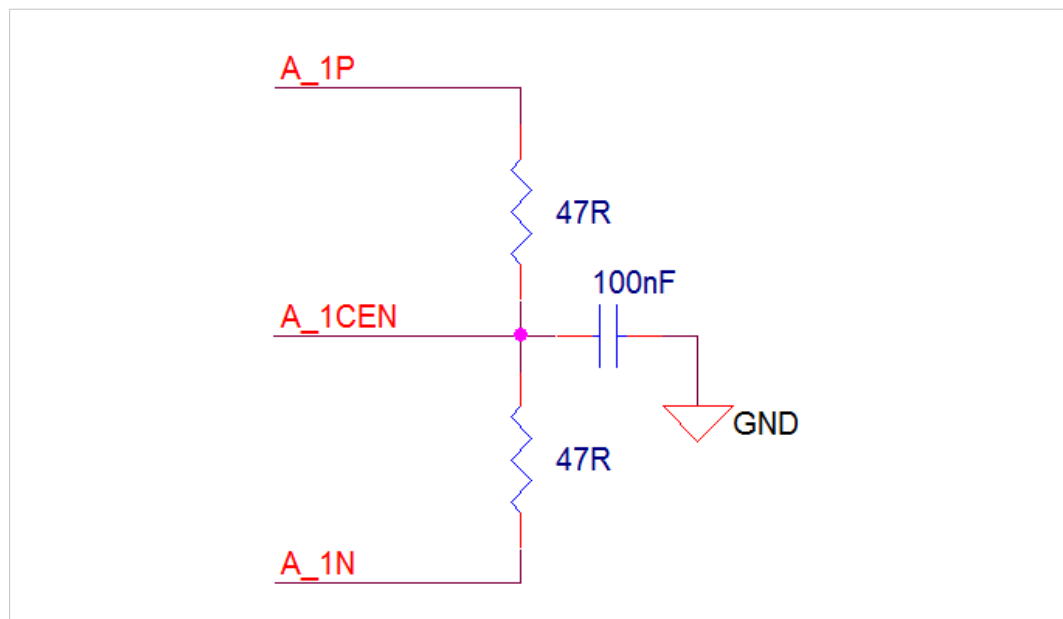
Fig. 24

Unused fibre optic connector pins should be connected as follows:

•   100R between TXP and TXN

•   820R between SDN and 3V3, resulting in 2 V on SDN

•   1k5 between SDP and 3V3, resulting in 1.5 V on SDP- Indicates that no signal is received. A signal amplitude of 0.5 V is appropriate.

•   4k7 between SCL and 3V3

•   4k7 between SDA and 3V3

Other network signals may be left floating when not used.

4.4   Ethernet Based Networks (Copper)

The industrial networks, that use Ethernet for communication, share the same hardware design. However, the firmware downloaded to the brick is different depending on network. Physically they use the same set of pins in a similar way. Bricks are available for the following Ethernet based networks: EtherNet/IP, EtherCAT. PROFINET, Ethernet POWERLINK, CC-Link IE Field and Modbus TCP.

The brick supports dual network ports, signal group A should be connected to the left port (port 1) and signal group B to the right port (port 2) on the connector board, looking at the front, see *Connector Board for Copper Based Ethernet, p. 55*

For EtherCAT, signal group A is used for the IN port and signal group B is used for the OUT port.

Signal Group	Signal Name	Type	Pin	Description
B	B_1P	I/O	3	First pair, positive signal
	B_1CEN	Power	4	Center tap voltage for first pair
	B_1N	I/O	5	First pair, negative signal
	B_2P	I/O	7	Second pair, positive signal
	B_2CEN	Power	8	Center tap voltage for second pair
	B_2N	I/O	9	Second pair, negative signal
	B_3P	I/O	11	Third pair, positive signal. Used for Gigabit Ethernet.
	B_3CEN	Power	12	Center tap voltage for third pair. Used for Gigabit Ethernet.
	B_3N	I/O	13	Third pair, negative signal. Used for Gigabit Ethernet.
	B_4P	I/O	15	Fourth pair, positive signal. Used for Gigabit Ethernet.
	B_4CEN	Power	16	Center tap voltage for fourth pair. Used for Gigabit Ethernet.
	B_4N	I/O	17	Forth pair, negative signal. Used for Gigabit Ethernet.
A	A_1P	I/O	29	First pair, positive signal
	A_1CEN	Power	30	Center tap voltage for first pair
	A_1N	I/O	31	First pair, negative signal
	A_2P	I/O	33	Second pair, positive signal
	A_2CEN	Power	34	Center tap voltage for second pair
	A_2N	I/O	35	Second pair, negative signal
	A_3P	I/O	37	Third pair, positive signal. Used for Gigabit Ethernet.
	A_3CEN	Power	38	Center tap voltage for third pair. Used for Gigabit Ethernet.
	A_3N	I/O	39	Third pair, negative signal. Used for Gigabit Ethernet.
	A_4P	I/O	41	Fourth pair, positive signal. Used for Gigabit Ethernet.
	A_4CEN	Power	42	Center tap voltage for fourth pair. Used for Gigabit Ethernet.
	A_4N	I/O	43	Forth pair, negative signal. Used for Gigabit Ethernet.

4.5   Ethernet Fiber Optic Networks

Ethernet fiber optic networks use more or less the same pins as copper based Ethernet networks. The brick supports PROFINET fiber optic network (PROFINET IRT).

The brick supports dual network ports, signal group A is be connected to the left port (port 1) and signal group B to the right port (port 2)on the connector board, looking at the front, see *Connector Board for Fiber Optic Ethernet, p. 56*.

If the Anybus CompactCom B40 connector board is not to be used, please study the design requirements for the Rx and SD channels, see *Rx Channel Design Requirements, p. 45* and *SD Channel Design Requirements, p. 46*. Furthermore, fiber optic connectors without metal are preferred in order to minimize EMC disturbance.

Signal Group	Signal Name	Type	Pin	Description
B	B_RXP	I	3	Rx, LVPECL positive signal
	B_SDA	I/O	4	SDA, I2C data
	B_RXN	I	5	Rx, LVPECL negative signal
	B_SDP	I	7	Signal Detect, LVPECL positive signal
	B_SCL	I/O	8	SCL, I2C clock
	B_SDN	I	9	Signal Detect, LVPECL negative signal
	B_TXEN	O	11	Tx enable TXEN is implemented as the inverse to TXDIS
	B_TXDIS	O	13	Tx disable
	B_TXP	O	15	Tx, LVPECL positive signal
	B_TXN	O	17	Tx, LVPECL negative signal
A	A_RXP	I	29	Rx, LVPECL positive signal
	A_SDA	I/O	30	SDA, I2C data
	A_RXN	I	31	Rx, LVPECL negative signal
	A_SDP	I	33	Signal Detect, LVPECL positive signal
	A_SCL	I/O	34	SCL, I2C clock
	A_SDN	I	35	Signal Detect, LVPECL negative signal
	A_TXEN	O	37	Tx enable TXEN is implemented as the inverse to TXDIS
	A_TXDIS	O	39	Tx disable
	A_TXP	O	41	Tx, LVPECL positive signal
	A_TXN	O	43	Tx, LVPECL negative signal

The differential signals Rx and Tx should be routed as differential pairs with a characteristic impedance of 100 Ω differentially.

4.5.1   Rx Channel Design Requirements

The Rx channel is designed for an optical transceiver output that has an AC coupled 100 Ω differential signal with 100-1000 mV amplitude, e.g. LVPECL (low voltage positive emitter coupled logic). Each line is terminated with 50 Ω to a common point with a potential of 1.2 V on the brick.

If a transceiver with a DC coupled output is used, series capacitors are needed to obtain desired signal levels for the brick. Below is a figure describing three different options to connect a transceiver output to an Rx channel on the brick:
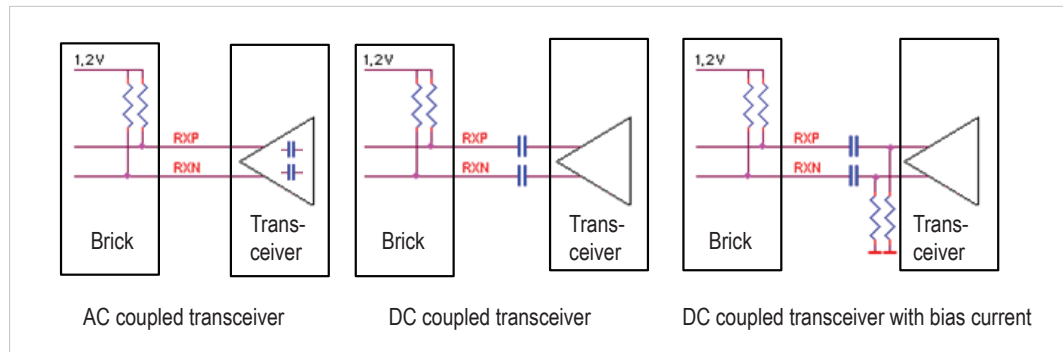
Fig. 25

The AC coupling capacitors typically have a value of 100 nF. Resistors draining bias current typically have a value of 150 Ω.

4.5.2   SD Channel Design Requirements

The SD (signal detect) channel is designed for a transceiver output that has a DC coupled differential output with 100-1000 mV amplitude. If a transceiver with LVTTL/LVCMOS output is used, the signal needs to be conditioned using a few resistors, to obtain desired signal levels for the brick.

Each line is pulled to GND by a 1.27 kΩ resistor on the brick.

Even if the transceiver has a single ended output and the other line is at a fixed reference potential, it is recommended to route SDN and SDP side by side all the way to the signal conditioning resistors. This will give the interference, collected by the transmission line, common mode characteristics, and it can thus be ignored by the differential input, instead of becoming a differential mode interference that would corrupt the signal.

Below is a figure describing three different ways to connect a transceiver output to an SD channel of the brick:
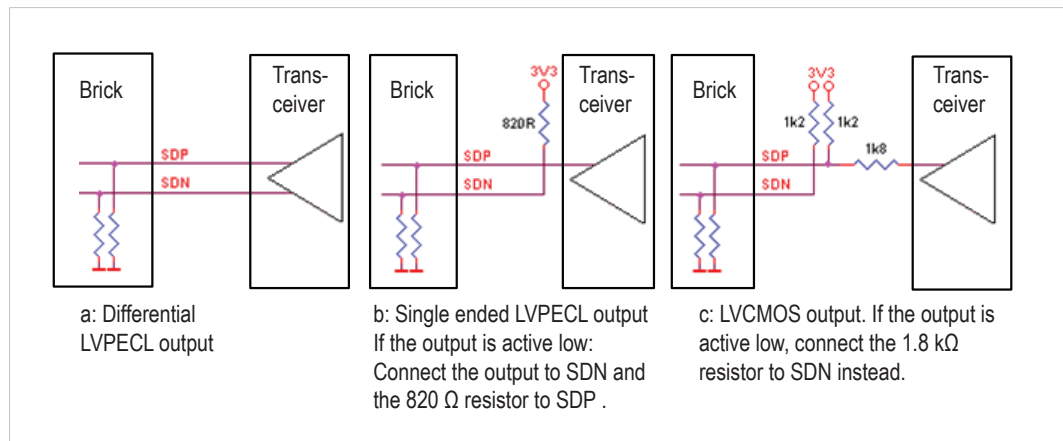
Fig. 26

In case a and case b, additional pull-down resistors will be required if the LVPECL outputs require a certain bias current (> 1 mA) to function.

4.6 DeviceNet

The Anybus CompactCom B40-1 DeviceNet communication interface uses the following pins:

Signal Name	Type	Pin	Description
C_TX	O	45	Tx
C_RX	I	46	Rx
C_BUSP_N	I	48	Bus power detection. Active low
GATE1	O	49	Low voltage MOS gate driver. For fieldbus isolated DC supply circuitry. The signals should preferably be routed to the connector board for future compatitibility, but for DeviceNet, the isolated circuitry is generally supplied by the bus power.
GATE2	O	50	

For mechanical drawing of the applicable connector board see: *Connector Board for CC-Link and DeviceNet, p. 57*

4.7 PROFIBUS

The Anybus CompactCom B40-1 PROFIBUS DP-V1 communication interface uses the following pins:

Signal Name	Type	Pin	Description
C_TX	O	45	Tx
C_RX	I	46	Rx
C_TXEN	O	47	TxEnable
GATE1	O	49	Low voltage MOS gate driver. For fieldbus isolated DC supply circuitry.
GATE2	O	50	Low voltage MOS gate driver. For fieldbus isolated DC supply circuitry.

For mechanical drawing of the applicable connector board see: *Connector Board for PROFIBUS, p. 54* for information about the optional connector board.

4.8 CC-Link

The Anybus CompactCom B40-1 CC-Link communication interface uses the following pins:

Signal Name	Type	Pin	Description
C_TX	O	45	Tx
C_RX	I	46	Rx
C_TXEN	O	47	TxEnable
GATE1	O	49	Low voltage MOS gate driver. For fieldbus isolated DC supply circuitry.
GATE2	O	50	Low voltage MOS gate driver. For fieldbus isolated DC supply circuitry.

For mechanical drawing of the applicable connector board see: *Connector Board for CC-Link and DeviceNet, p. 57* for information about the optional connector board.

4.9   LED Indicators

The Anybus CompactCom 40 series supports four bicolored LED indicators.

LED name	Pin no.	Signal Name	Default color	Default Functionality	
LED1	26	NW_LED1A	Green	Network status	
	25	NW_LED1B	Red		
LED2	24	NW_LED2A	Green	Module status	
	23	NW_LED2B	Red		
LED3	22	NW_LED3A	Green	All Industrial Ethernet Networks:	Link/Act for the network port (port A)
				Other:	Not used
	21	NW_LED3B	Yellow	EtherNet/IP, Modbus-TCP	10 Mbit Link/Act for Link/Act for the network port (port A)
				Other	Not used
LED4	20	NW_LED4A	Green	All Industrial Ethernet Networks:	Link/Act for the network port (port B)
				Other:	Not used
	19	NW_LED4B	Yellow	EtherNet/IP, Modbus-TCP	10 Mbit Link/Act for Link/Act for the network port (port B)
				Other	Not used

All LED outputs are active high and should be connected as shown in the picture below. The resistor values should be chosen to get even light between different LEDs.

Fig. 27

4.9.1   Ethernet, 1000 Mbit

For Gigabit Ethernet applications, another solution for connecting the LEDs is needed to obtain indications equal to the Anybus CompactCom M40. The solution, presented here, can be used for 10 and 100 Mbit applications as well. The table below shows how to interpret the LED indications in this case.

> (i) *Please note that the only Anybus CompactCom 40 that at this time supports 1 Gbit communication over Ethernet, is the Anybus CompactCom 40 CC-Link IE Field.*

LEDxA	LEDxB	Indication
Low	Low	Off
Low	High	Yellow LED on for link detected, flickers to indicate 10 Mbit activity
High	Low	One green LED on for link detected, flickers to indicate 100 Mbit activity
High	High	Two green LEDs on for link detected, flickers to indicate 1 Gbit activity

All LED outputs are active high and should be connected as shown in the picture below.
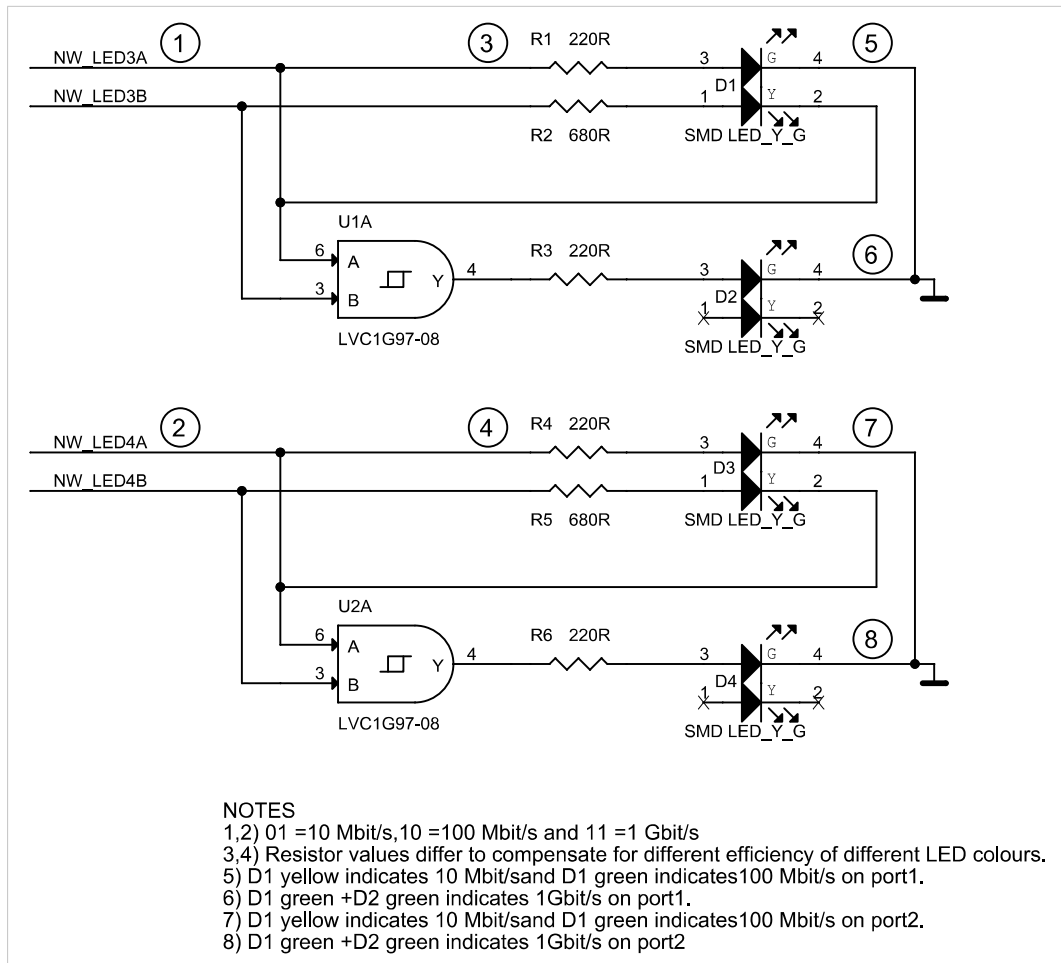
Fig. 28

5　EMC

This section offers information, necessary when designing in an Anybus CompactCom B40-1, to ensure sufficient performance related to EMC. However, an engineering assessment is always needed to ensure the quality. HMS Industrial Networks does not leave any guarantees, but provides relevant information to the customers.

5.1　General

When working with a design in relation to EMC, it is recommended to always aim for good signal integrity, since this is highly related to the EMC. For power, this means solid planes for both power and GND together with good decoupling between the planes. As the quality of the power is of great importance, it is important to perform sufficient verifications during the design process to ensure this. This is also true for signals, where good signal integrity most likely results in good EMC performance. There should always exist good connection to a reference plan without any obstacles for the return current. Traces should also be kept short, with as few board and cable transitions as possible, since every transition will have a negative impact on the signal integrity.

For GND planes, the following basic design rules are important:

- A continuous and stable GND plane is needed underneath the B40 connectors in order to ensure good signal integrity.

- The plane must follow the signal path through the connector

Considering the host application connector, different protocols are more sensitive to interference than others. E.g. try to avoid using parallel and RMII interface in the design, if the recommendations in this section cannot be followed or if the risk of interference is high. To ensure stability, there has to be a sufficient separation on the host board between a parallel interface and an RMII interface.

5.2　Bulk and Decoupling

Recommendations regarding bulk and decoupling capacitors is presented in *Bypass Capacitance, p. 73*.

The capacitors have impact on the power quality at the Anybus CompactCom board, but are also of importance in relation to EMC immunity. These general recommendations should be evaluated for every design. The values may also need to be adjusted in relation to power consumption, power quality on the main board, and the layout of the main board.

5.3　Reset Signal

There are several aspects to consider when routing the reset signal for the Anybus CompactCom. Requirements for rise and fall time, but also the relation between the power up and the reset signal are described in *RESET (Reset Input), p. 18*. These requirements must be met in all designs to ensure stability. If the reset signal has a long trace or if there is any other aspect that has a negative impact on the signal integrity, an RC filter may be required. To minimize the risk of EMC problems, it is possible to add footprints for a RC-filter in advance and evaluate the need before it becomes a problem during any certification. When designing the filter, all timing aspects must be considered, so that the timing requirements in *RESET (Reset Input), p. 18* are fulfilled.

6 Black Channel/Safety Interface

The black channel is a transportation mechanism for safety related protocol extensions over a nonsafe communication media. The safety layer performs safety related transmission functions and checks on the communication to ensure that the integrity of the link meets the requirement for SIL 3, cat4/PL e. The black channel can be seen as a virtual link between the safety layers of the devices.
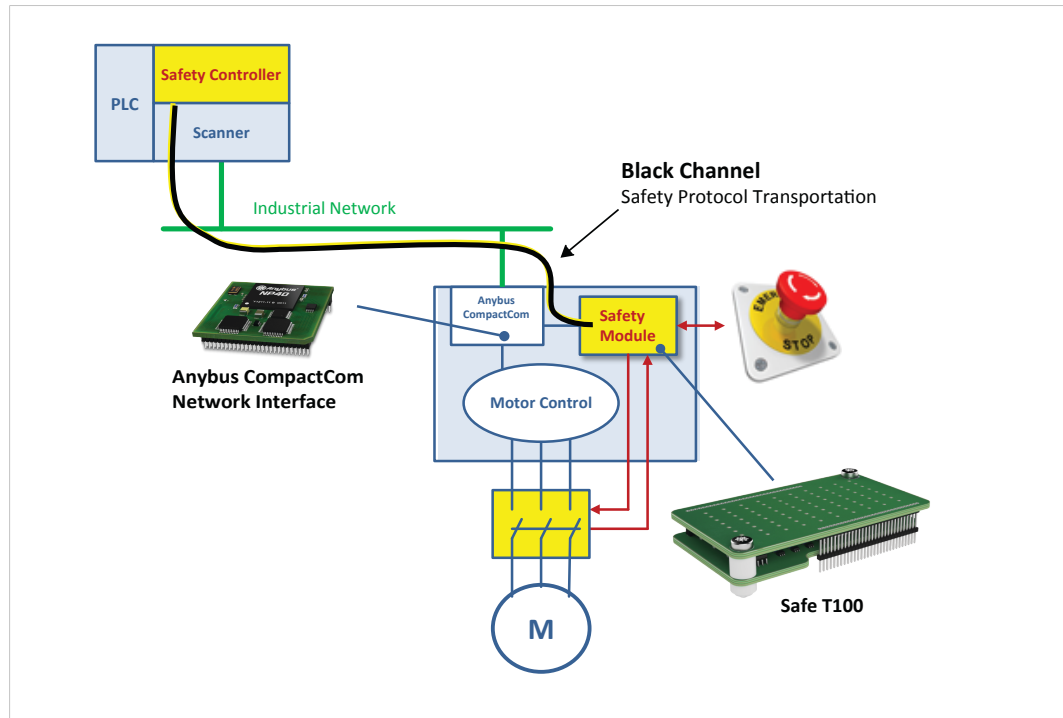
Fig. 29

The IXXAT Safe T100 is a precertified embedded safety option module which provides device manufacturers with an easy and cost efficient way to integrate conformant safe I/O signals into standard automation devices. It connects via its serial black channel interface to the Anybus CompactCom module. The safety module provides digital safe I/O signals that can be controlled via the network and that can be directly connected to the safety functions of an automation device. Other standard safety modules can also be used to provide a safety communication interface for the Anybus CompactCom 40 series.

The same serial interface is used both for serial download and for safety communication. Please take this in account when implementing the use of a safety module or Black Channel.

A   Mechanical Specification

> ❗ This a class A product. In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate measures.
>
> This product contains ESD (Electrostatic Discharge) sensitive parts that may be damaged if ESD control procedures are not followed. Static control precautions are required when handling the product. Failure to observe this may cause damage to the product.

All dimensions are in millimeters, tolerance ±0.10 mm, unless otherwise stated.

A.1   Anybus CompactCom B40-1

The dimensions for the Anybus CompactCom B40-1 are given in the picture below.
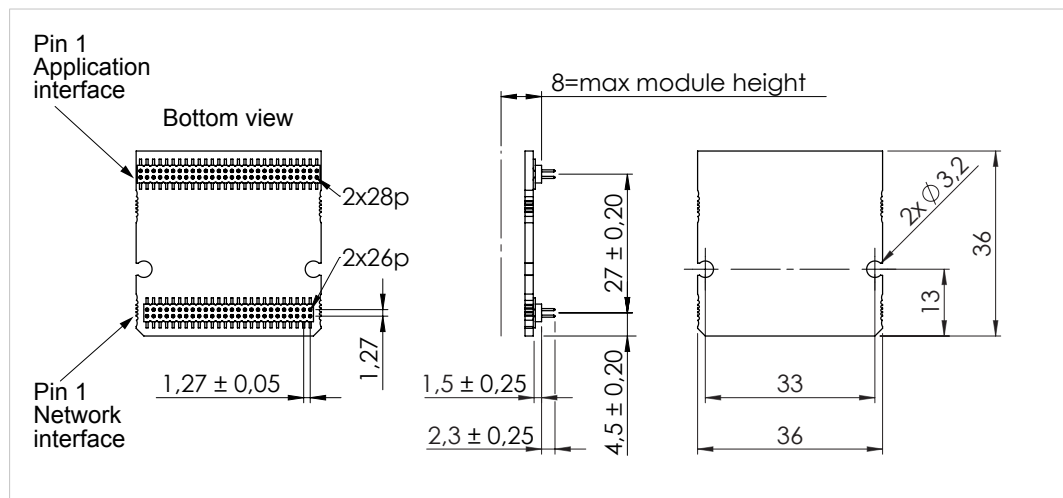
Fig. 30

A.2   Connector Board for PROFIBUS

The connector board for the PROFIBUS network interface carries a D-sub connector

> ❗ If the connector board is mounted in an environment that is subject to vibration, please make sure to secure the network cable in such a manner, that the vibrations will not harm the D-sub connector.
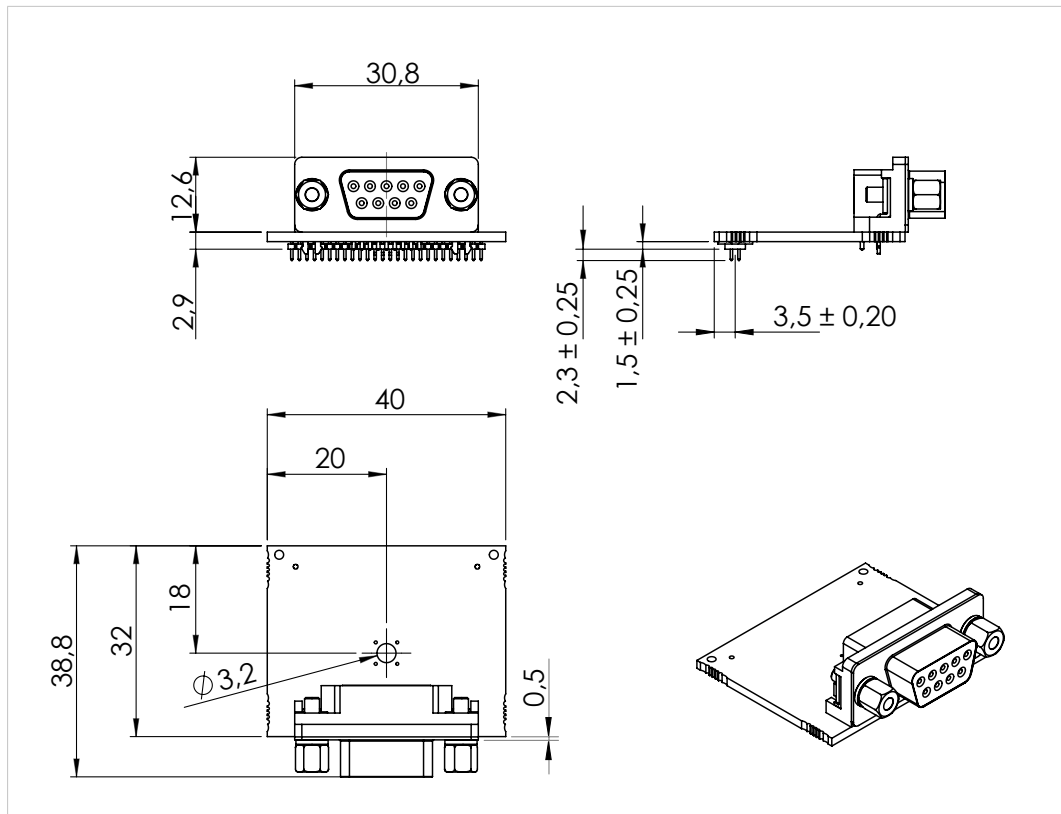
Fig. 31

A.3   Connector Board for Copper Based Ethernet

The connector board for the copper based Ethernet network interfaces carries two RJ45 connectors.
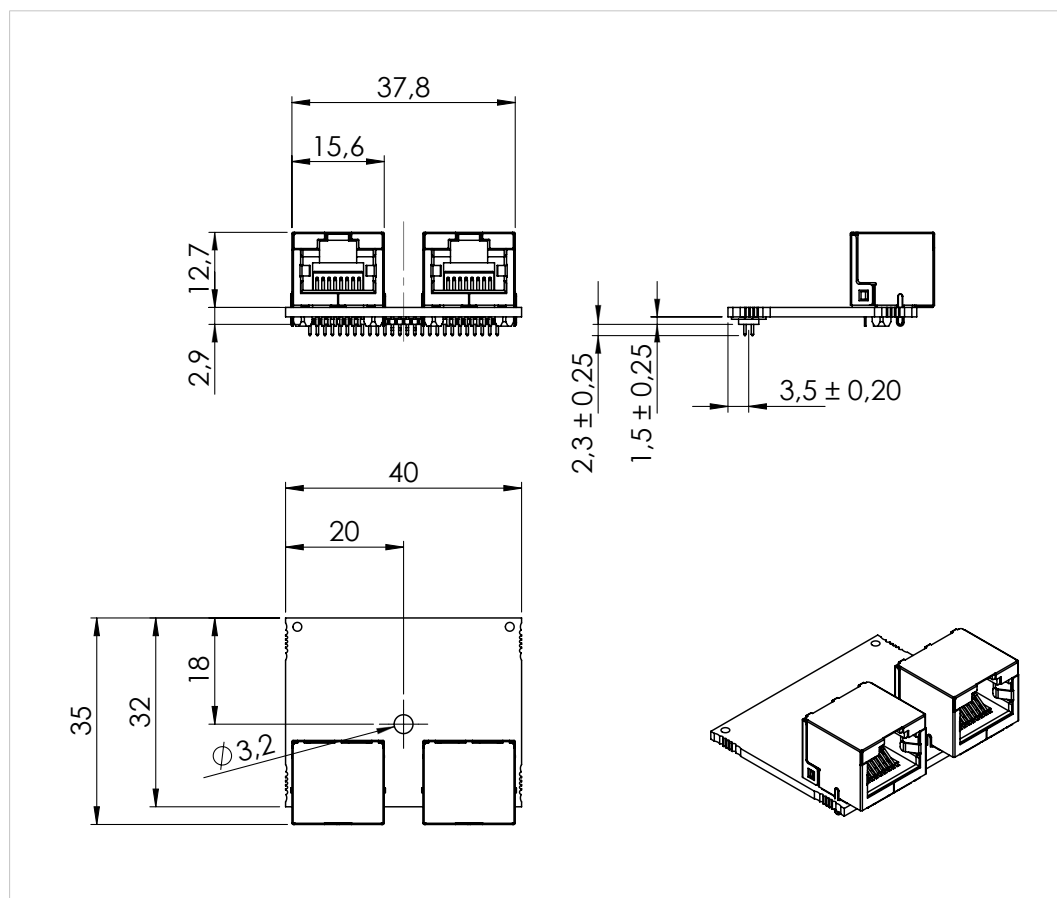
Fig. 32

A.4   Connector Board for Fiber Optic Ethernet

The connector board for the Fiber Optic Ethernet network interface carries two fibre optic transceivers.
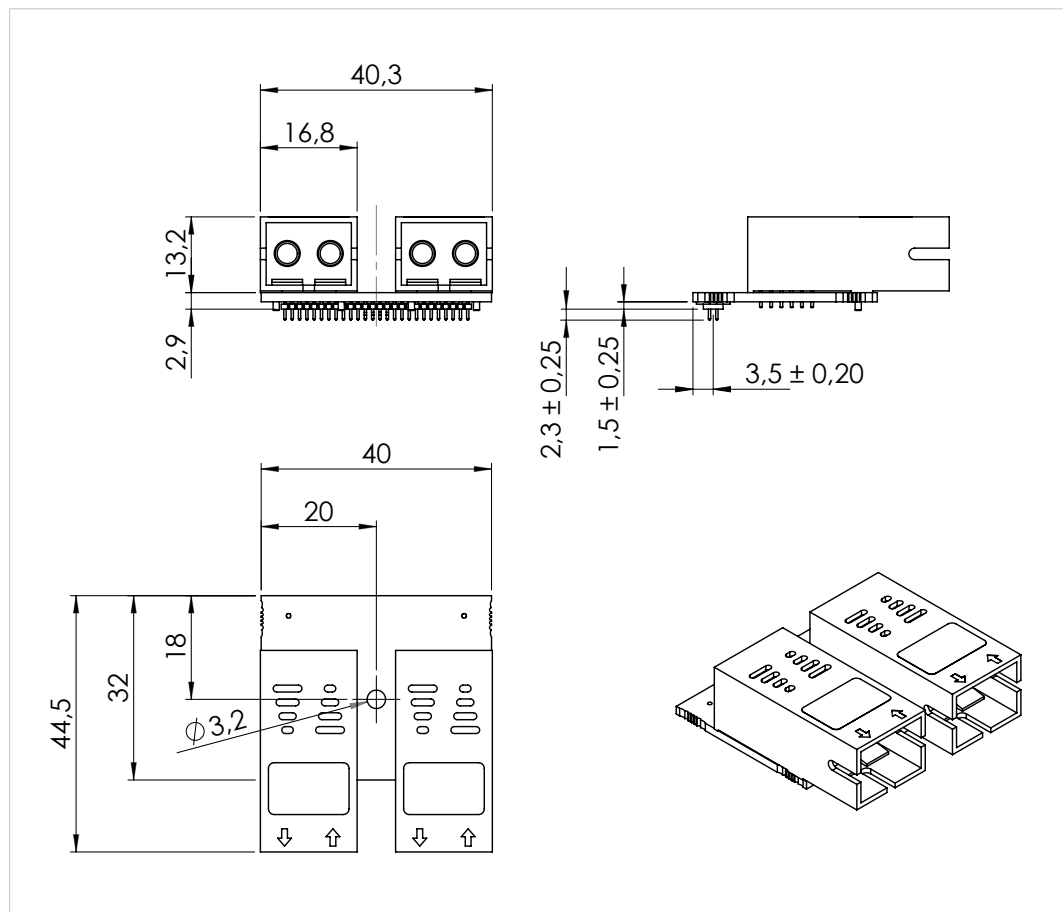
Fig. 33

A.5   Connector Board for CC-Link and DeviceNet

The connector board for the CC-Link and the DeviceNet network interfaces carry a pluggable
screw terminal (5.08mm)
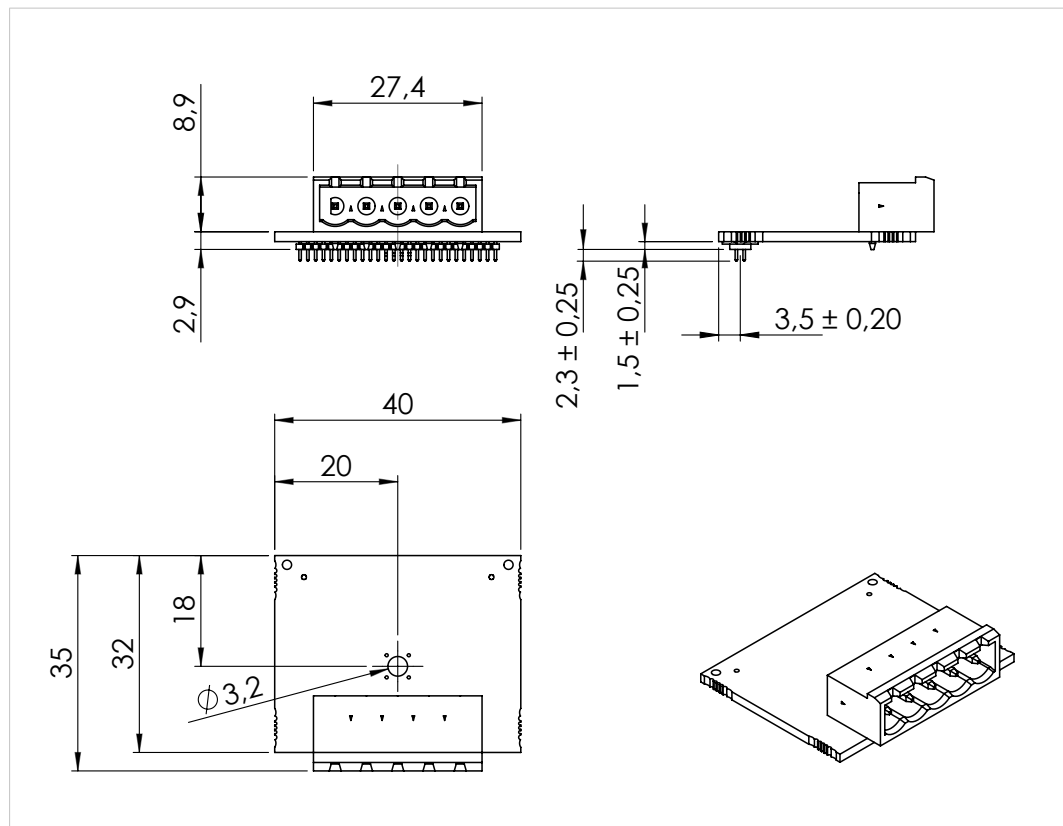
Fig. 34

A.6   Footprints

A.6.1   Anybus CompactCom B40-1

The Anybus CompactCom B40-1 is connected to the host application board through the host application interface connector and a network interface connector. The footprint for the Anybus CompactCom B40-1 is shown in the picture below.
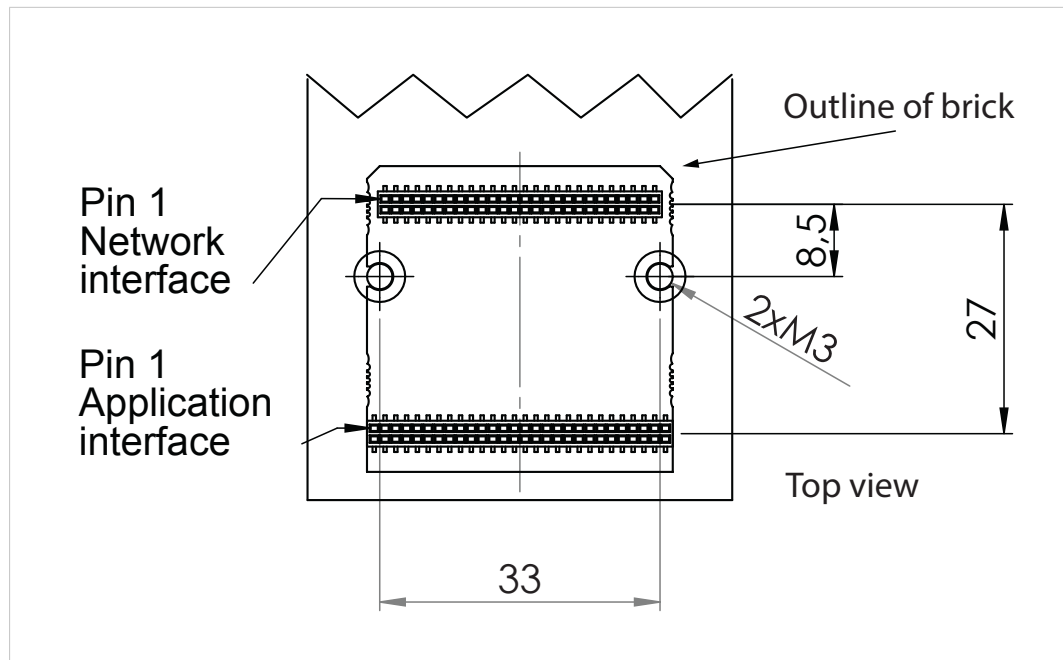
Fig. 35

See *Assembly, p. 60* for suggested components.

A.6.2 Network Connector Board

The network connectors are mounted on a separate connector board. The footprint for a connector board is shown in the figure below. This footprint is the same for all connector boards
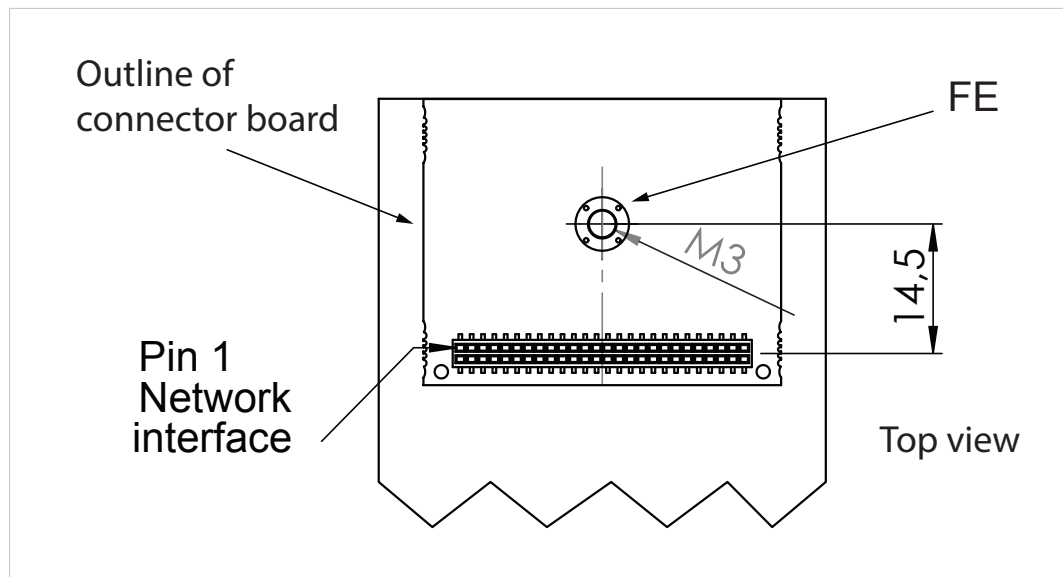
Fig. 36

The fastening screw must be connected to the functional earth (FE) of the host application.

See for suggested components.

A.7 Height Restrictions

All dimensions are in millimeters
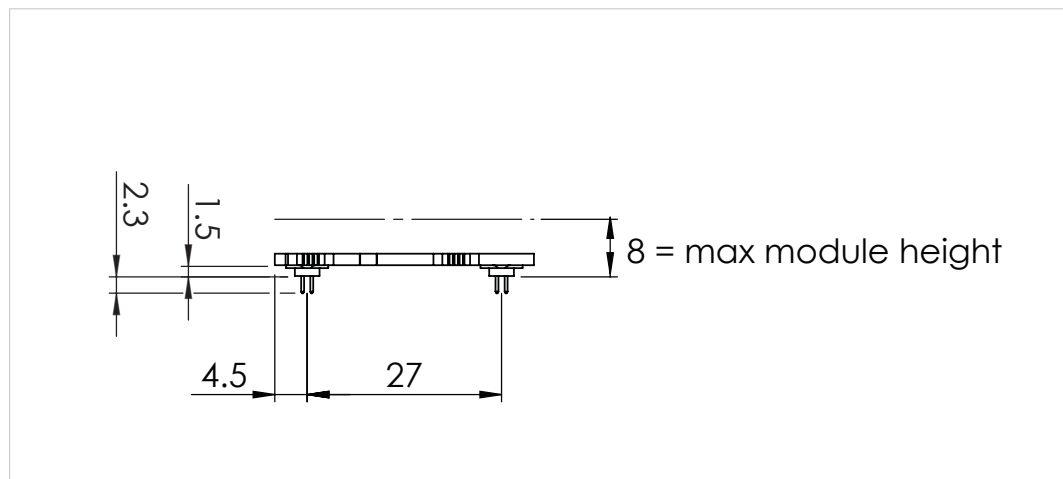
Fig. 37

(i) *The maximum height occupied by onboard components of the Anybus module is 8 mm. To ensure isolation, it is recommended to add an additional 2.5 mm on top of these dimensions.*

A.8   Front Plate Restrictions

Customer applications that have a front plate with hole(s) for accessing the connector(s) of a connector board, must have the front plate placed at least 0.5 mm away from the connector board edge and must not reach further than 2.5 mm away from the connector board edge.
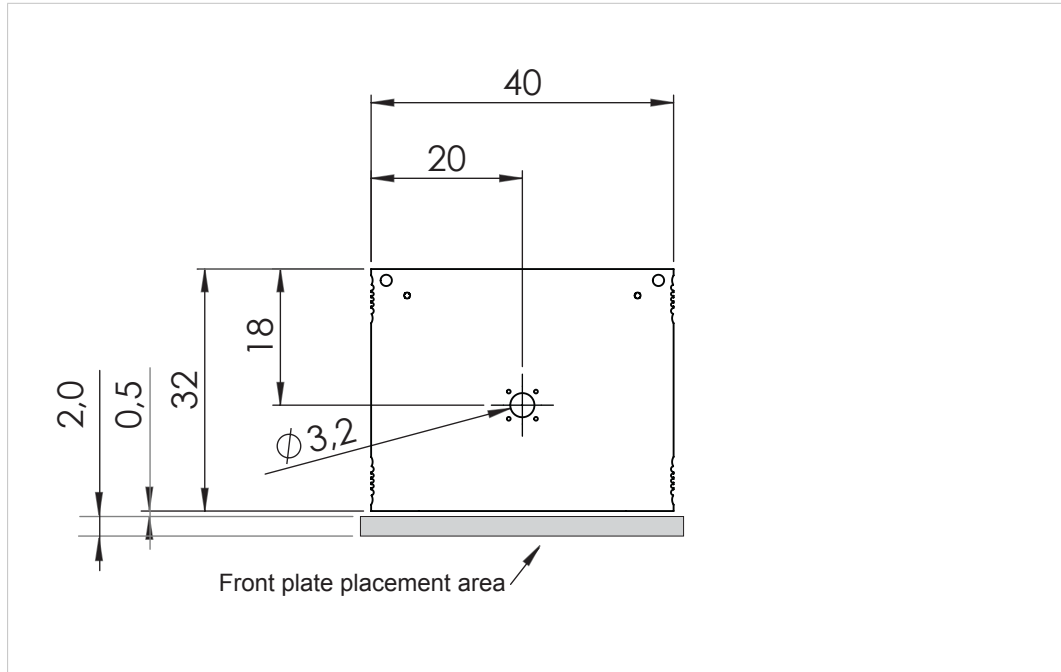
Fig. 38

A.9   Assembly

The Anybus CompactCom B40-1 and the connector board are mounted separately on to the host application board. The connector board has to be secured using a screw, joining FE (functional earth) on the connector board to FE on the host application board. The screw holes of the Anybus CompactCom B40-1 are not connected to FE, but to GND. If suggested components are used, the Anybus CompactCom B40-1 can be mounted without screws in a low vibration environment, see *Shock and Vibration, p. 63* for more information.

The Anybus CompactCom B40-1 can either be connected to the application board using headers, or soldered directly to the host application PCB.
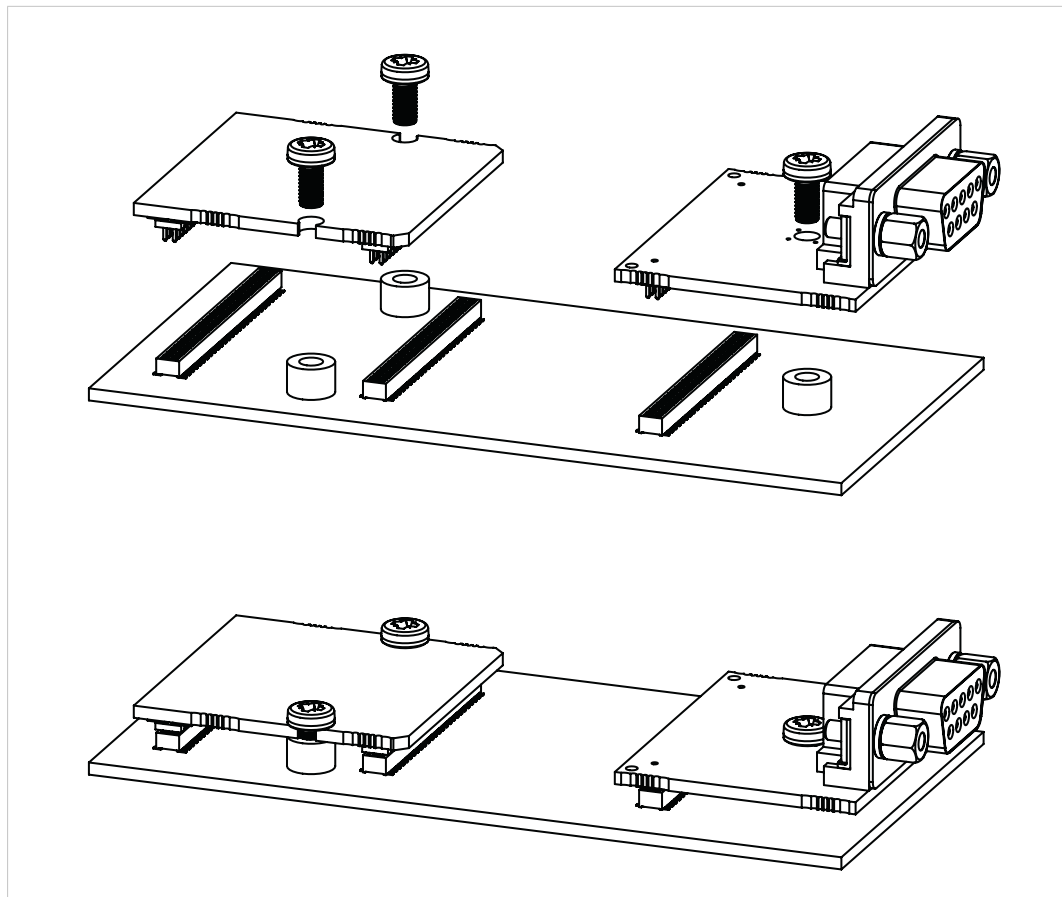
Fig. 39

Suggested components		
Header	Application interface	Samtec CLP-128-02-L-D (56 pin)
	Network interface	Samtec CLP-126-02-L-D (52 pin)
Stand-off (M3)	Pemnet SMTSO-M3-4-ET	

The screw standoffs are typically 4 mm tall. If the Anybus CompactCom B40-1 and connector board are to be soldered directly to the host application board, standoffs should be 2 mm tall. Outer diameter may be 6 mm max. The standoffs should not extend outside the screw mount pads.

Recommended torque is 0.2 Nm. Locking paint kan be used to secure the screws against loosening.

PCB layout

Outline of
connector board

FE

M3

14,5

Pin 1
Network
interface

Top view

Standoffs, typ. 4 mm

Outline of brick

Pin 1
Network
interface

8,5

27

Pin 1
Application
interface

2xM3

Top view

33

M3: Standoff with internal thread, size M3
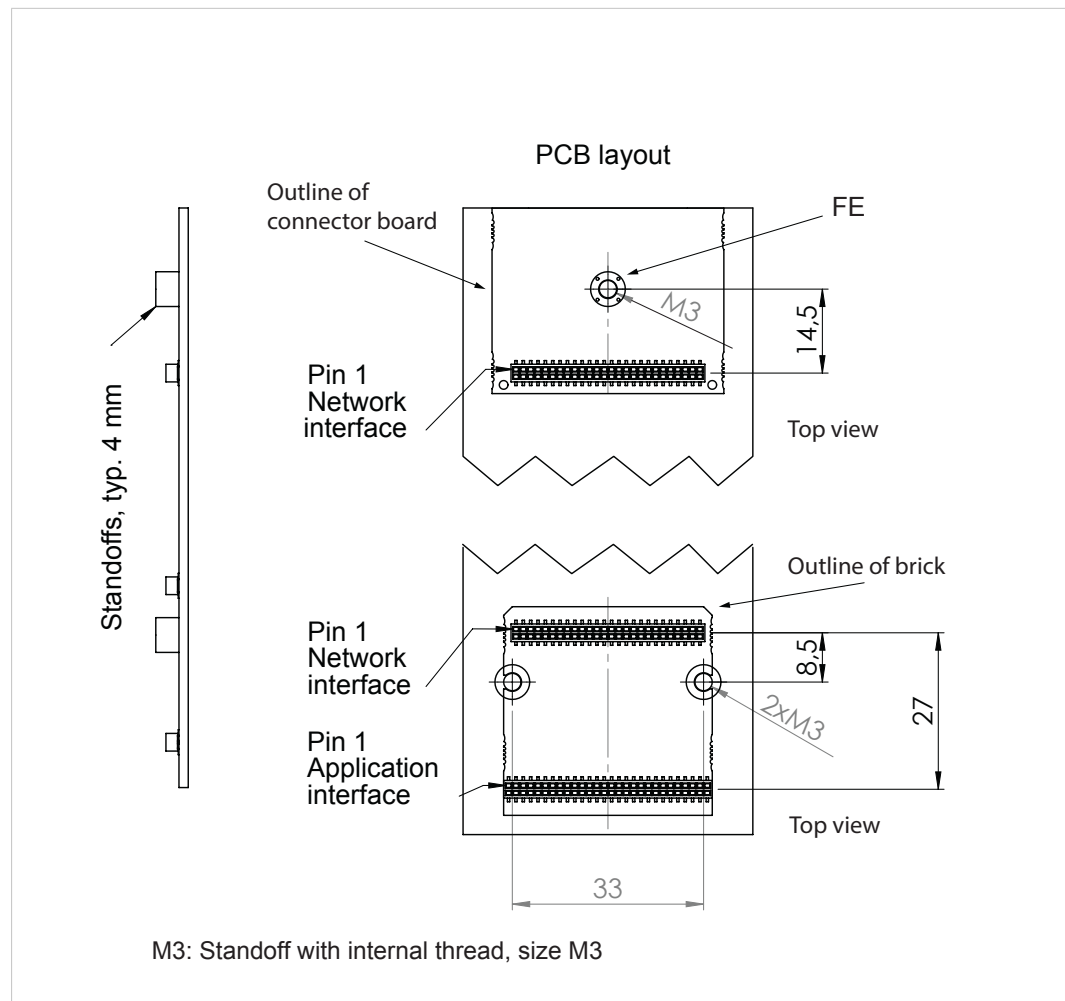
Fig. 40

B Technical Specification

B.1 Environmental

B.1.1 Operating

-40 to 85° C (-40 to 185° F)

B.1.2 Storage

-40 to 85°C (-40 to 185° F)

B.1.3 Humidity

5 to 95% non-condensing

B.2 Shock and Vibration

B.2.1 Shock

The Anybus CompactCom B40-1 is tested according to IEC 68–2–27

- half-sine 30 g, 11 ms, 3 positive and 3 negative shocks in each of three mutually perpendicular directions

- half-sine 50 g, 11 ms, 3 positive and 3 negative shocks in each of three mutually perpendicular directions

Connector boards/interface cards are tested for 30 g.

B.2.2 Sinusoidal Vibration

The Anybus CompactCom B40-1 is tested according to IEC 68–2–6

Frequency range:	10–500 Hz
Amplitude 10–49 Hz:	0.35 mm
Acceleration 50–500 Hz	5 g
Sweep rate:	1 oct/min
	10 double sweep in each of the three mutually perpendicular directions

B.3 Electrical Characteristics

> ! Failure to follow the requirements may lead to permanent hardware damage

It is recommended for Anybus CompactCom B40-1 users to make sure that each signal controlling the Anybus CompactCom B40-1 has a drive strength enough to fulfill level and timing constraints even if the signal is loaded with 20 pF in parallel with 2.2 kΩ to GND or 3V3.

B.3.1   Operating Conditions

Symbol	Parameter	Pin Types	Conditions	Min.	Typ.	Max.	Unit
3V3	Supply Voltage (DC)			3.15	3.30	3.45	V
	Ripple (AC)			-	-	± 100	mV
GND	Ground reference		-	0.00	0.00	0.00	V
I_{IN}	Current consumption (also including network interfaces and network status LEDs)	PWR	Class A	-	-	250	mA
			Class B	-	-	500	mA
			Class C	-	-	1000	mA
V_{IH}	Input High Voltage	I, BI	-	2.0	-	3.45	V
V_{IL}	Input Low Voltage			-0.3	-	0.8	V
I_{OH}	Current, Output High	O, BI	-	-8.0	-	8.0	mA
I_{OL}	Current, Output Low						
V_{OH}	Output High Voltage		I_{OH} = -4mA	2.4	-	-	V
V_{OL}	Output Low Voltage		I_{OL} = 4mA	-	-	0.4	V
I_{OH} (NW_LEDx)	Output Current , network LEDs	O				20	mA

I= Input, CMOS (3.3V)

O= Output, CMOS (3.3V)

BI= Bidirectional, Tristate

PWR= Power supply inputs

B.4   Regulatory Compliance

EMC Compliance (CE)

Since the Anybus CompactCom is considered a component for embedded applications it cannot be CE-marked as an end product.

However the Anybus CompactCom 40 family is pre-compliance tested in a typical installation providing that all modules are conforming to the EMC directive in this installation.

The EMC pre-testing has been conducted according to the following standards:

Emission: EN61000-6-4	EN55016-2-3 Radiated emission
	EN55022 Conducted emission
Immunity: EN61000-6-2	EN61000-4-2 Electrostatic discharge
	EN61000-4-3 Radiated immunity
	EN61000-4-4 Fast transients/burst
	EN61000-4-5 Surge immunity
	EN61000-4-6 Conducted immunity

Since all Anybus CompactCom B40-1 modules have been evaluated according to the EMC directive through above standards, this serves as a base for our customers when certifying Anybus CompactCom B40-1 based products.

C   How to Disable Ethernet Port 2 (EtherNet/IP)

It is possible to disable Ethernet Port 2 on the Anybus CompactCom B40-1 EtherNet/IP.

- Do not connect signal group B
- Do not connect signals LED4A/B

> **!** It is not possible to disable Ethernet Port 2 on any other Anybus CompactCom B40-1 than EtherNet/IP.

For descriptions of signals see:

- *Overview, p. 41*
- *Ethernet Based Networks (Copper), p. 44*
- *LED Indicators, p. 48*

D Implementation Examples

D.1 General

In this appendix HMS Industrial Networks provides examples of possible implementations for the Anybus CompactCom B40-1 series.

There are many different processors with different functionality available on the market today. The implementations in this appendix are to be regarded as examples that are designed for one single type of processor. Other hardware interfaces may require adjustments for timing, different functionality etc. It is important to fully understand the interface to take correct design decisions in order to obtain a stable and reliable design.

D.2 SPI

This design is intended for an SPI implementation.
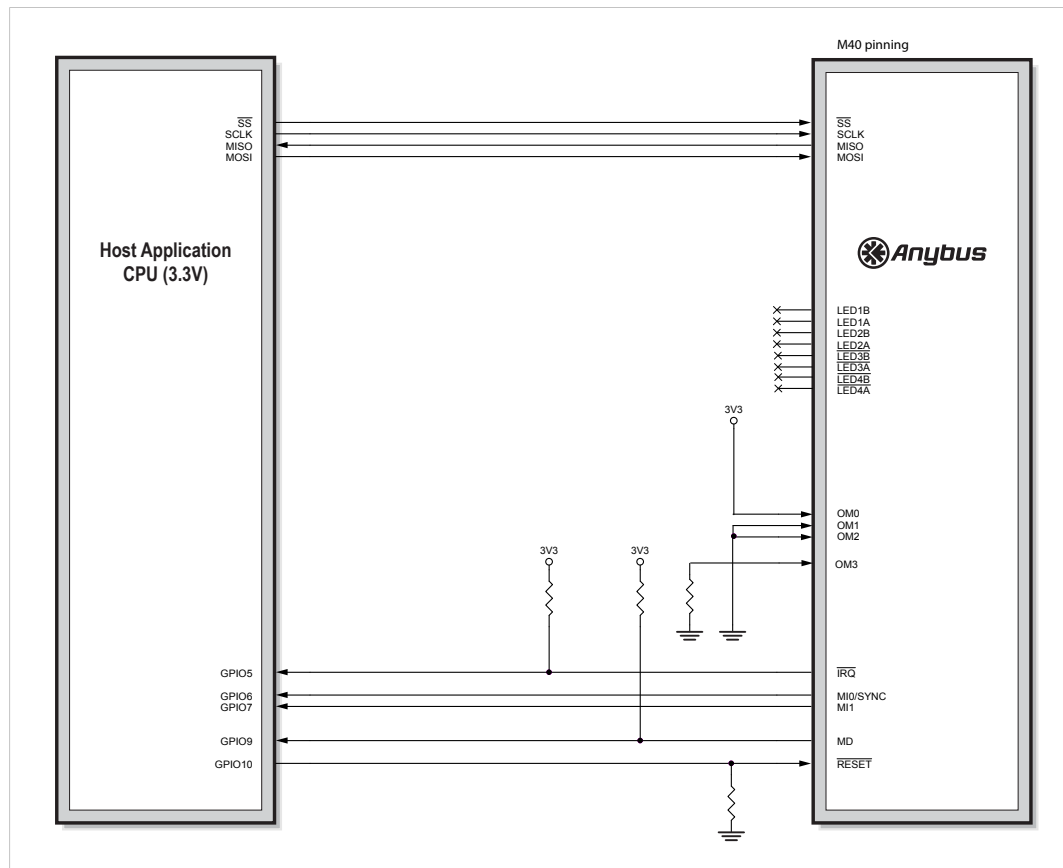
Fig. 41

If LEDs are to be used in the host application, please refer to *Network Status LED Outputs (LED [1A...4B]), p. 70*, for guidelines on how to connect the LED outputs.

D.3 16-bit Parallel

This example shows a design for 16-bit parallel mode.
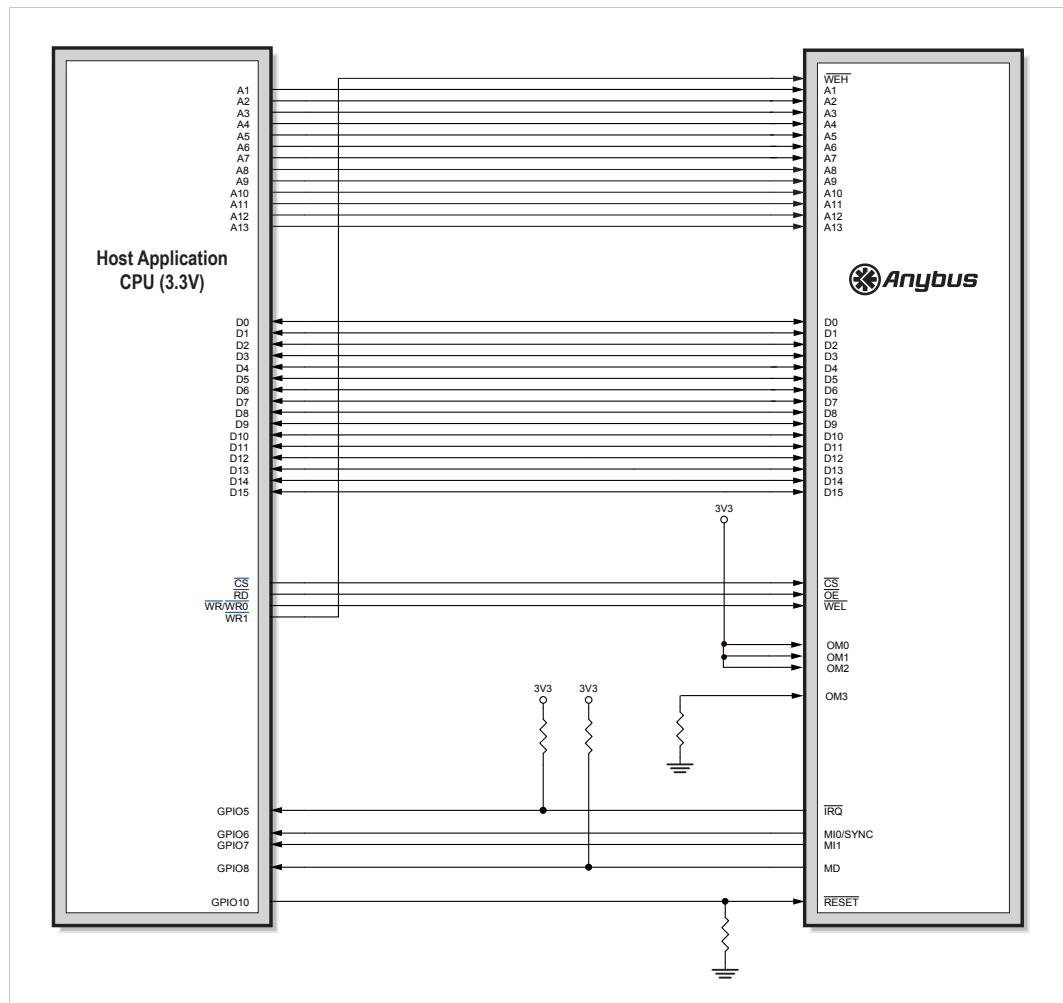
Fig. 42

If LEDs are to be used in the host application, please refer to *Network Status LED Outputs (LED [1A...4B]), p. 70*, for guidelines on how to connect the LED outputs. In 16-bit parallel mode it is not possible to use these outputs for LEDs. The network status LED signals are always present on the network interface connector, see *Network Connector, p. 40*.

D.4 8-bit Parallel

This design is intended for 8-bit parallel mode.

Fig. 43

If LEDs are to be used in the host application, please refer to *Network Status LED Outputs (LED [1A...4B]), p. 70*, for guidelines on how to connect the LED outputs.

D.5 Serial

The example in the figure below shows an implementation with serial communication.
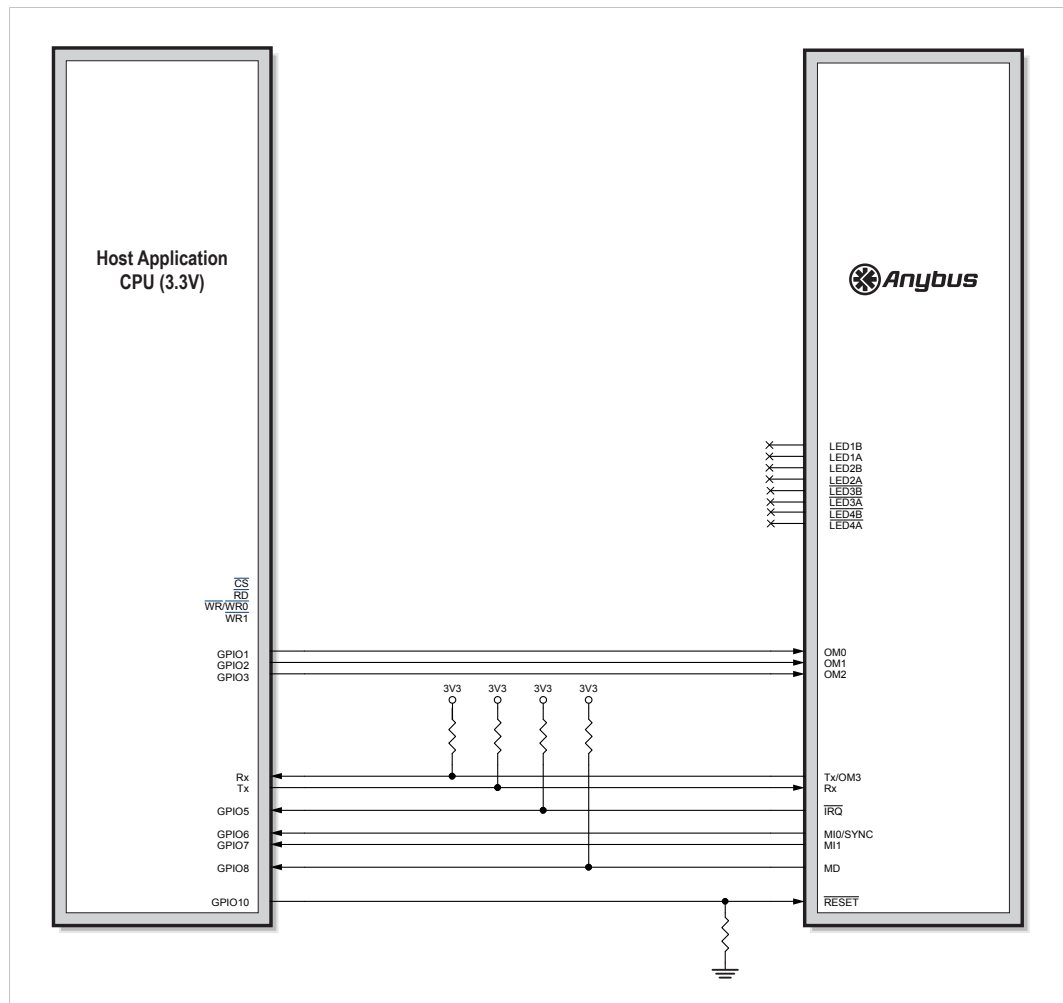
Fig. 44

D.6 Network Status LED Outputs (LED[1A...4B])

All network status LED signals are easily available on the network interface connector. It is recommended to use these signals when the network status is to be displayed. However they are also available on the host interface connector (LED[1A...4B]).

The LED[1A....4B] outputs can be used to relay the network status LEDs to elsewhere on the host application. This is possible in all modes except 16-bit parallel mode, where these pins are used for data (D8...D15).

Note that it is the responsibility of the host application to ensure that each LED output is connected to a LED of the correct color (it is possible to retrieve this information from the LED status register or from the Anybus Object (01h); consult the Anybus CompactCom Software Design Guide for more information). For more information, see *LED Interface / D8–D15 (Data Bus), p. 14*.

The outputs are unbuffered, and are not recommended for driving LEDs directly. Please consult the image below for guidelines on how to connect the LED outputs.

*By connecting this signal to Ground, this design can be used to support Anybus CompactCom passive modules.
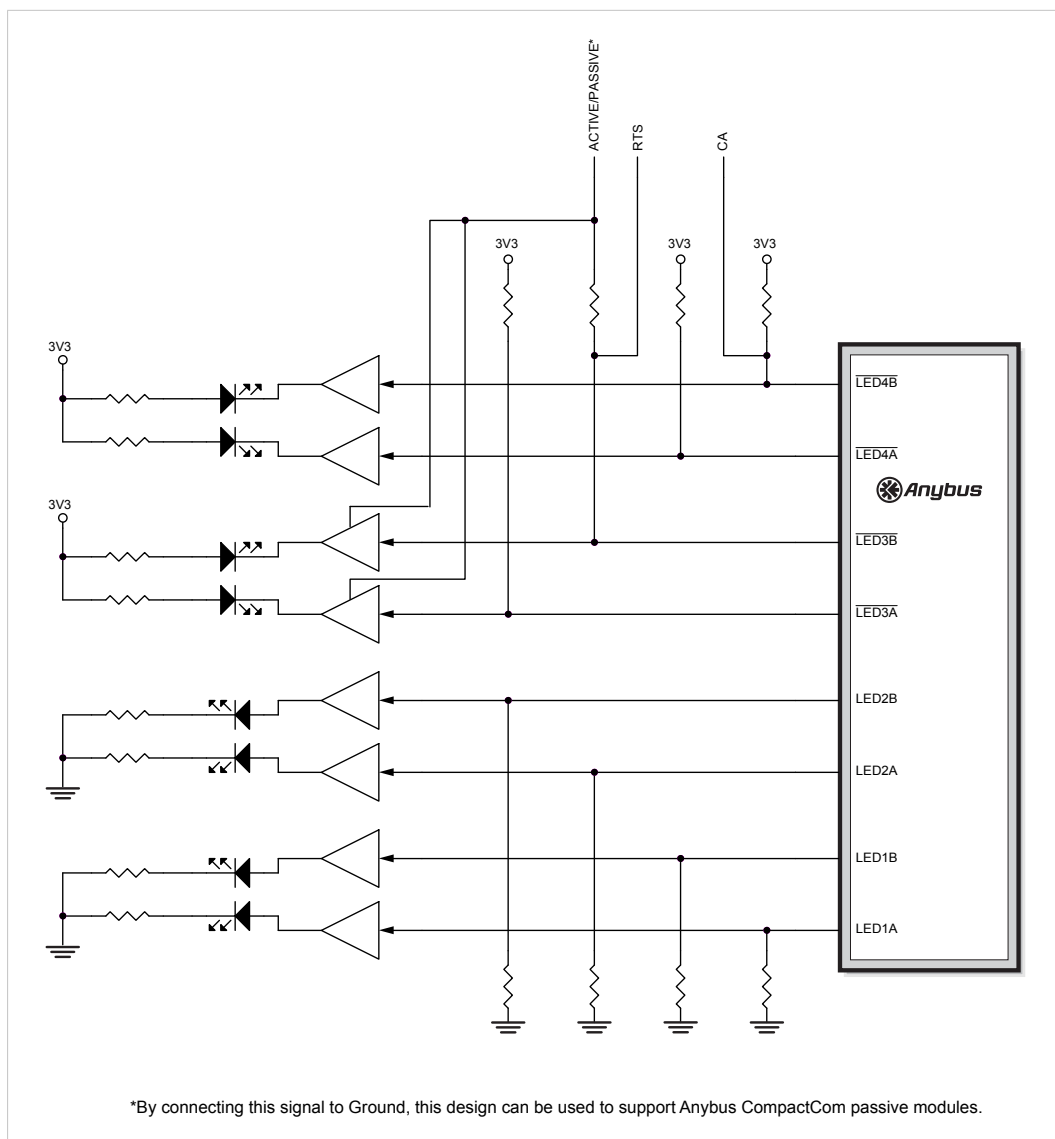
Fig. 45

ⓘ *These pins can not be used for LEDs in 16-bit parallel mode, as the pins in that case are used for data. All network status LED signals are present on the network interface connector, and can be connected from there.*

D.7   Power Supply Considerations

D.7.1   General

The Anybus CompactCom 40 platform in itself is designed to be extremely power efficient. The exact power requirements for a particular networking system will however vary a lot depending on the components used in the actual bus circuitry.

While some systems usually require less than 250 mA of supply current at 3.3 V, some high performance networks, or networks which require the use of legacy ASIC technology, will consume up to 500 mA, or in rare cases even as much as 1000 mA.

As an aid when designing the power supply electronics, the networks have been divided into classes based on their power consumption as follows.

• Class A: less than 250 mA

• Class B: up to 500 mA

• Class C: up to 1000 mA

Please note that the power supply classifications take into account that the power budget is shared with a full fieldbus circuitry, e.g. the appropriate connector board and NW_LEDs with maximized consumption (20 mA each).

The following table lists the currently supported networking systems and their corresponding class.

Network	Class A	Class B	Class C
DeviceNet		X	
PROFIBUS	X		
CANopen	X		
EtherCAT		X	
PROFINET 2-Port		X	
PROFINET FO 2-Port			X
Ethernet/IP 2-Port		X	
EtherNet POWERLINK		X	
Common Ethernet		X	
CC-Link		X	
Modbus-TCP 2-Port		X	
CC-Link IE Field			X
BACnet/IP		X	

A power supply designed to fulfill Class A requirements (250 mA), will be able to support all networks belonging to class A, but none of the networks in Class B and C.

A power supply designed to fulfill Class C requirements, will be able to support all networks.

D.7.2 Bypass Capacitance

The power supply inputs must have adequate bypass capacitance for high-frequency noise suppression. It is therefore recommended to add extra bulk capacitors near preferably all the power supply inputs (or at least two):

Reference	Value (Ceramic)
C1	10 µF / 6.3 V
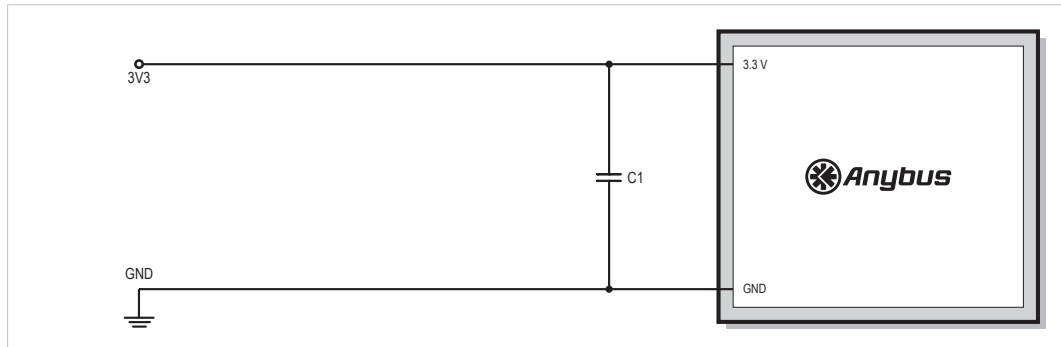
Fig. 46

D.7.3 3.3 V Regulation

The following example uses the LT1767 from Linear Technology to provide a stable 3.3 V power source for the module. Note that all capacitors in this example are of ceramic type.
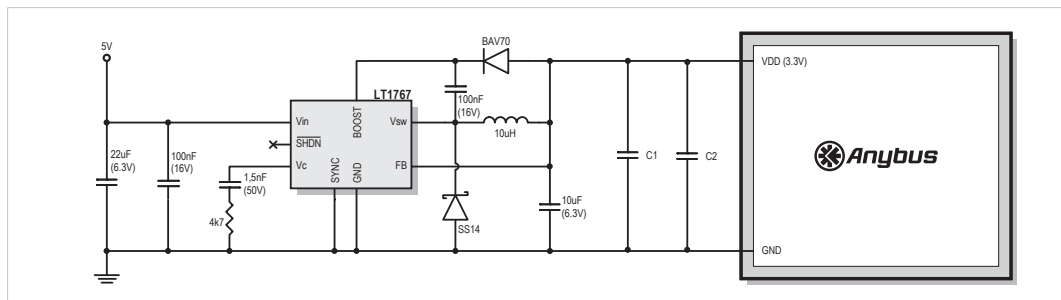
Fig. 47

ⓘ *For detailed information regarding this example, consult the data sheet for the LT1767 (Linear Technology).*

E   Design Examples, Network Interface

If the optional connector board is used, the signals from the network interface connector of the brick can be routed directly to the corresponding pins of the connector on the connector board. Section *E.2* shows an example PCB layout for this case.

This appendix also contains typical examples, of how to design the network interface, if the optional connector board is not to be used. See *Network Interface Examples, p. 77*.

E.1   Recommendations

- The longer the distance between the Brick and the Connector board, the more important it is that single-ended signals as well as signal pairs are separated from other signals and signal pairs to maintain good signal integrity.

- All conductors should have a tighter coupling to a continuous ground plane than to any adjacent conductor (even to the partner signal of a signal pair). All signal pairs should have a differential impedance of 100 Ω ±10%.

  It is not recommended to separate network circuitry, e.g. Connector board, and Brick more than 400 mm. The distance should be kept shorter if the signals are adjacent to other interfering circuitry. Radiated interference from the signals between the Connector board and Brick may need to be taken care of by e.g. a metallic housing or encapsulating PCB copper planes if the routing distance is long.

- If a design will be used for Gigabit Ethernet applications, the following has to be fulfilled:

  – The maximum difference in length, between signal pairs (1 - 4) in the design must not exceed 6.7 mm.

  – The maximum difference in length, between the two signals in a signal pair must not exceed 0.25 mm from Phy to Gigabit Magnetics and 0.25 mm from Gigabit Magnetics to the Ethernet connector.
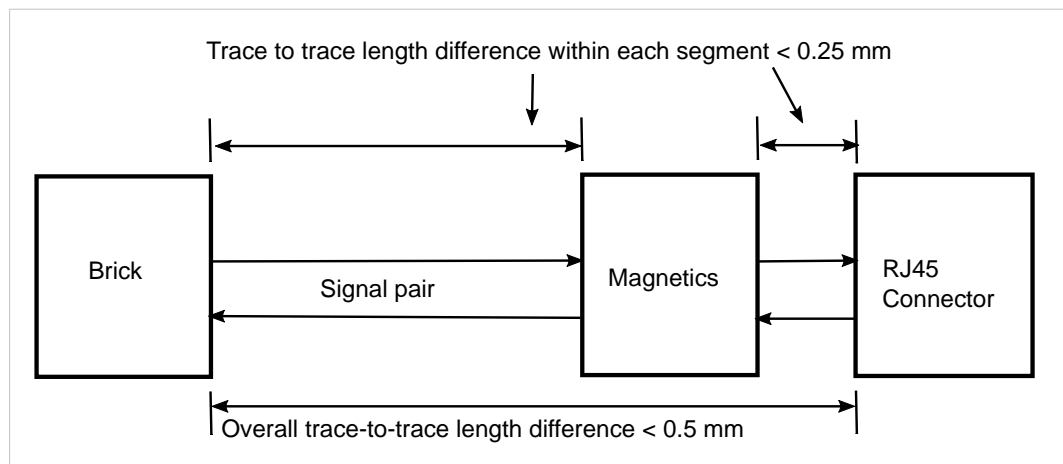
Fig. 48

- To avoid B40-1 connector pins penetrating the solder mask under the headers on the carrier board, thus creating short circuits, the following is recommended:

  – either use headers that are higher than 2.5 mm,

  – or do not design any vias or traces on top side of the PCB, where there is any risk for short circuits, see figure in section *E.2*.

- Minimum recommended power rating for termination/grounding resistors is 1/16 W.

- DC/DC transformer selection recommendations:
    - 1:2.1 turns ratio
    - 500 kHz switching frequency
    - The transformer shall be able to deliver at least 100 mA on the network interface side without saturating, at Anybus CompactCom min/max supply voltage, and at the relevant min/max ambient temperature that is applicable
    - Under the above circumstances, the transformer and rectifier output voltage must allow the regulator tokeep the 5V rail inside a ±5% tolerance

E.2 PCB Layout

The pin headers of the Anybus CompactCom B40-1 have pins which are 2.3 mm tall nominally, but to avoid risk of short circuit when the pin length is in the upper tolerance region, it is suggested to have via/route keepouts on the PCB top layer, in between the pad rows, as the figure shows, unless a receptacle taller than 2.6 mm is used.
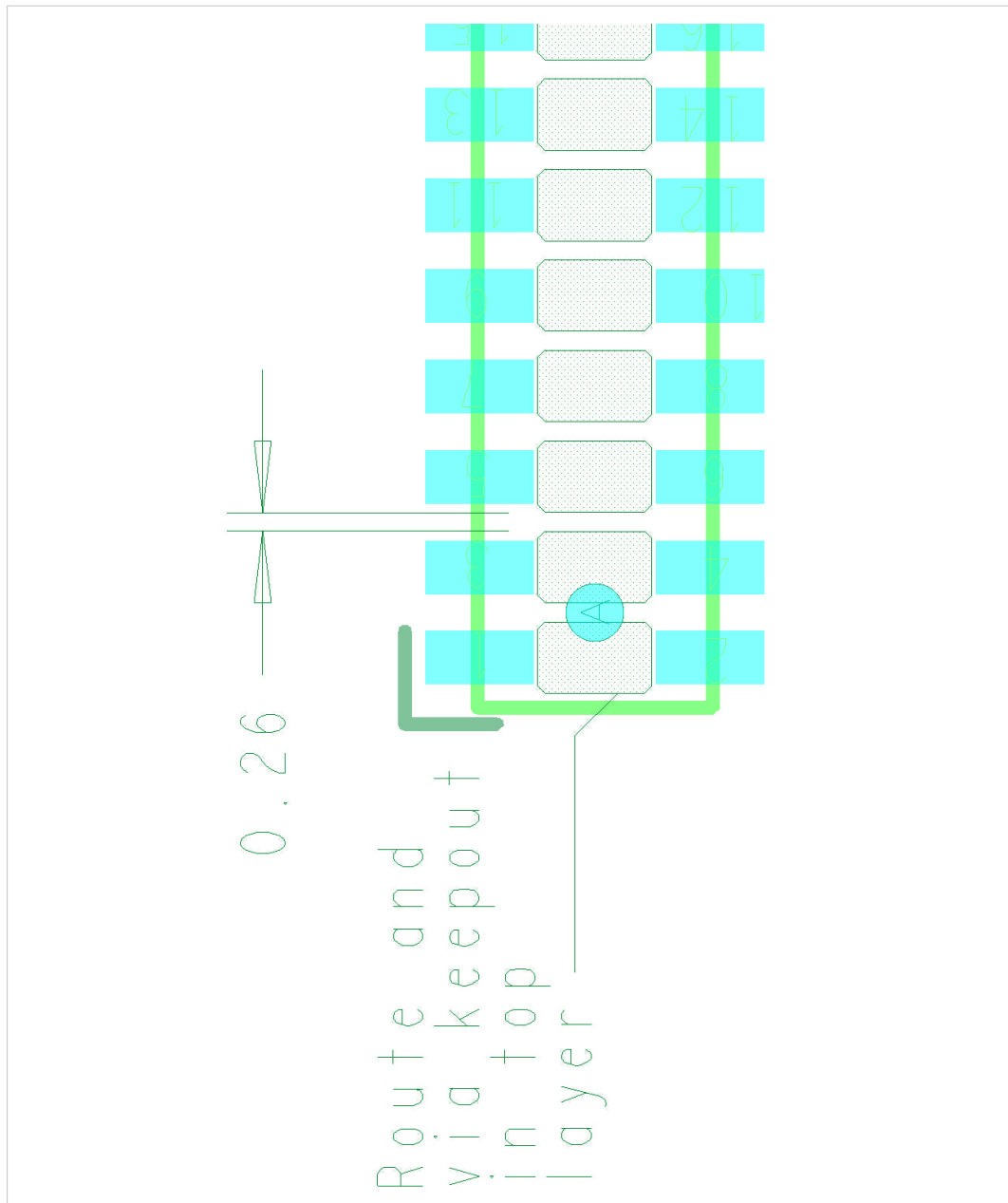
Fig. 49

E.3   Network Interface Examples

This section contains typical examples, of how to design the network interface, if the optional connector board is not to be used. Examples are given for the usual network connectors as well as for M12 connectors making a higher IP rating possible.

Example Schematics	Brick	Comments
10 and 100 Mbit Ethernet Network Interface(Copper)	EtherNet/IP EtherCAT Modbus TCP Common Ethernet POWERLINK PROFINET IRT BACnet/IP	All bricks for 100 Mb/s Ethernet based protocols, running on copper wire, use the same hardware. Ethernet trafo example: 7490100111A (Würth Elektronik Gmbh) RJ45 connector example: SS-60300-032 (Bel stewart)
100 Mbit Ethernet Network Interface (Fiber Optic)	PROFINET IRT	-
10 and 100 Mbit Ethernet Network Interface (M12)	EtherNet/IP EtherCAT Modbus TCP Common Ethernet POWERLINK PROFINET IRT BACnet/IP	All bricks for 100 Mb/s Ethernet based protocols, running on copper wire, use the same hardware. Ethernet trafo example: 7490100111A (Würth Elektronik Gmbh)
10, 100 and 1000 Mbit Ethernet Network Interface	CC-Link IE Field	RJ45 connector example: SS-60300-032 (Bel stewart)
PROFIBUS	PROFIBUS	-
PROFIBUS (M12)	PROFIBUS	-
DeviceNet	DeviceNet	-
DeviceNet (M12)	DeviceNet	-
CC-Link	CC-Link	-
CANopen	CANopen	-

Design Example
10 and 100 Mbit Ethernet
Network Interface
with RJ-45 connectors

J6

1 3V3
2
3 B_1P/RXP
4 B_1CEN/SDA
5 B_1N/RXN
6
7 B_2P/SDP
8 B_2CEN/SCL
9 B_2N/SDN
10
11 B_3P/TXEN
12 B_3CEN/RX
13 B_3N/TXDIS
14
15 B_4P/TXP/TX
16 B_4CEN/CD/BUSP_N
17 B_4N/TXN/TX_N
18
19 NW_LED4B_N
20 NW_LED4A_N
21 NW_LED3B_N
22 NW_LED3A_N
23 NW_LED2B_N
24 NW_LED2A_N
25 NW_LED1B_N
26 NW_LED1A_N
27 3V3
28
29 A_1P/RXP
30 A_1CEN/SDA
31 A_1N/RXN
32
33 A_2P/SDP
34 A_2CEN/SCL
35 A_2N/SDN
36
37 A_3P/TXEN
38 A_3CEN/RX
39 A_3N/TXDIS
40
41 A_4P/TXP/TX
42 A_4CEN/CD/BUSP_N
43 A_4N/TXN/TX_N
44
45 C_TX
46 C_RX
47 C_TXEN
48 C_BUSP_N
49 GATE1
50 GATE2
51 3V3
52

B40-1 connector

TR2
Ethernet Trafo
7490100111A (Würth Elektronik Gmbh)

B_1P
B_1N
B_1CEN
B_2CEN
B_2P
B_2N

TDB+
TDB-

RDB+
RDB-

1
C2
100nF/16V

2
C3
100nF/16V

R2 75R   R3 75R   R4 75R   R5 75R

C4
1nF/2kV

FE

C1
1nF/2kV

R1
1M

FE

J5
TDB+ 1
TDB- 2
RDB+ 3
      4
      5
RDB- 6
      7
      8
      9
SHIELDB 10

1
2
3
4
5
6
7
8
9
10

RJ-45 connector
SS-60300-032 (Bel stewart)

TR1
Ethernet Trafo
7490100111A (Würth Elektronik Gmbh)

A_1P
A_1N
A_1CEN
A_2CEN
A_2P
A_2N

TDA+
TDA-

RDA+
RDA-

3
C6
100nF/16V

4
C7
100nF/16V

R8 75R   R9 75R   R6 75R   R10 75R

C8
1nF/2kV

FE

C5
1nF/2kV

R7
1M

FE

J4
TDA+ 1
TDA- 2
RDA+ 3
      4
      5
RDA- 6
      7
      8
SHIELDA 9
       10

1
2
3
4
5
6
7
8
9
10

RJ-45 connector
SS-60300-032 (Bel stewart)

Notes:
1,2,3,4) Place center tap capacitors close to the respective transformer.

Design Example
Ethernet Fibre Optics
Network Interface

3V3
J1, pin #1
C1
10uF/10V
C2
100nF/16V

J1

1	3V3
2	
3	B_1P/RXP
4	B_1CEN/SDA
5	B_1N/RXN
6	
7	B_2P/SDP
8	B_2CEN/SCL
9	B_2N/SDN
10	
11	B_3P/TXEN
12	B_3CEN/RX
13	B_3N/TXDIS
14	
15	B_4P/TXP/TX
16	B_4CEN/CD/BUSP_N
17	B_4N/TXN/TX_N
18	
19	NW_LED4B_N
20	NW_LED4A_N
21	NW_LED3B_N
22	NW_LED3A_N
23	NW_LED2B_N
24	NW_LED2A_N
25	NW_LED1B_N
26	NW_LED1A_N
27	3V3
28	
29	A_1P/RXP
30	A_1CEN/SDA
31	A_1N/RXN
32	
33	A_2P/SDP
34	A_2CEN/SCL
35	A_2N/SDN
36	
37	A_3P/TXEN
38	A_3CEN/RX
39	A_3N/TXDIS
40	
41	A_4P/TXP/TX
42	A_4CEN/CD/BUSP_N
43	A_4N/TXN/TX_N
44	
45	C_TX
46	C_RX
47	C_TXEN
48	C_BUSP_N
49	GATE1
50	GATE2
51	3V3
52	

3V3
R5
820R
2

B_SDN
B_SDP
B_RXN
B_RXP
B_TXP
B_TXN

C15
100nF/16V
C16
100nF/16V
R1
0R
2

B_SDPA
B_RXNA
B_RXPA

3V3
3V3

1

R3
150R
R4
150R

3V3
R10
4k7
R11
4k7
R12
4k7
R13
4k7

B_SDA
B_SCL
B_TXDIS

A_SDA
A_SCL
A_TXDIS

A_SDN
A_SDP
A_RXN
A_RXP
A_TXP
A_TXN

R6
820R
3V3

2

1

C17
100nF/16V
C18
100nF/16V
R2
0R

A_SDPA
A_RXNA
A_RXPA

3V3
3V3

R8
150R
R9
150R

Port B

U1
6 RD+
5 RD-
4 SD
3 RxVCC
2 RxGND
1 SDA
14 GND#14

7 TxVCC
8 TxGND
9 TxDIS
10 TD+
11 TD-
12 SCL
13 GND#13

QFBR-5978Z

Right port, seen from the front side

Port A

U2
6 RD+
5 RD-
4 SD
3 RxVCC
2 RxGND
1 SDA
14 GND#14

7 TxVCC
8 TxGND
9 TxDIS
10 TD+
11 TD-
12 SCL
13 GND#13

QFBR-5978Z

Left port, seen from the front side

3V3
J1, pin #51
C5
10uF/10V
C6
100nF/16V

3V3
U1, pin #3
C3
100nF/16V
C4
4u7F/6V3

3V3
U1, pin #7
C9
100nF/16V
C10
4u7F/6V3

3V3
U2, pin #3
C7
100nF/16V
C8
4u7F/6V3

3V3
U2, pin #7
C11
100nF/16V
C12
4u7F/6V3

Notes:
1) RX and TX signal pairs shall have a differntial impedance of 100 Ohm.
2) Do not mount R1, R2, R5 and R6 if SD interface is not used.

Design Example
10 and 100 Mbit Ethernet
Network Interface
with M12 connectors

J6

1 3V3
2
3 B_1P/RXP
4 B_1CEN/SDA
5 B_1N/RXN
6
7 B_2P/SDP
8 B_2CEN/SCL
9 B_2N/SDN
10
11 B_3P/TXEN
12 B_3CEN/RX
13 B_3N/TXDIS
14
15 B_4P/TXP/TX
16 B_4CEN/CD/BUSP_N
17 B_4N/TXN/TX_N
18
19 NW_LED4B_N
20 NW_LED4A_N
21 NW_LED3B_N
22 NW_LED3A_N
23 NW_LED2B_N
24 NW_LED2A_N
25 NW_LED1B_N
26 NW_LED1A_N

27 3V3
28
29 A_1P/RXP
30 A_1CEN/SDA
31 A_1N/RXN
32
33 A_2P/SDP
34 A_2CEN/SCL
35 A_2N/SDN
36
37 A_3P/TXEN
38 A_3CEN/RX
39 A_3N/TXDIS
40
41 A_4P/TXP/TX
42 A_4CEN/CD/BUSP_N
43 A_4N/TXN/TX_N
44
45 C_TX
46 C_RX
47 C_TXEN
48 C_BUSP_N
49 GATE1
50 GATE2
51 3V3
52

B40-1 connector

TR2
Ethernet Trafo
7490100111A (Würth Elektronik Gmbh)

B_1P
B_1N
B_1CEN
B_2CEN
B_2P
B_2N

TDB+
TDB-

RDB+
RDB-

1 C2
   100nF/16V
2 C3
   100nF/16V

R2 75R
R3 75R

C4 1nF/2kV

FE

TR1
Ethernet Trafo
7490100111A (Würth Elektronik Gmbh)

A_1P
A_1N
A_1CEN
A_2CEN
A_2P
A_2N

TDA+
TDA-

RDA+
RDA-

3 C6
   100nF/16V
4 C7
   100nF/16V

R8 75R
R9 75R

C8 1nF/2kV

FE

J5
RDB+ 2
TDB+ 1
RDB- 4
TDB- 3
SHIELDB 6
Female D-coded M12 connector

C1 1nF/2kV
R1 1M
FE

J4
RDA+ 2
TDA+ 1
RDA- 4
TDA- 3
SHIELDA 6
Female D-coded M12 connector

C5 1nF/2kV
R7 1M
FE

Notes:
1,2,3,4) Place center tap capacitors close to the respective
transformer.

Design Example
10, 100 and 1000 Mbit Ethernet
Network Interface

Notes:
1, 2) Center tap capacitors are placed close to respective transformer.
3, 4) Four differential pairs with impedance and length matching. Differential
        impedance is 100 ohm and length matching within 0,25 mm between and totally
        from J1 to TR1 and from TR1 to J2.
5, 6) Four differential pairs with impedance and length matching. Differential
        impedance is 100 ohm and length matching within 0,25 mm between and totally
        from J1 to TR2 and from TR2 to J3.
7, 8) Pairs A, B, C and D are length matched in between. Max length difference between
        the longest and the shortest pair is 6,7 mm from J1 to J2.
9, 10) Pairs A, B, C and D are length matched in between. Max length difference between
        the longest and the shortest pair is 6,7 mm from J1 to J3.
11, 12) No routing under magnetics.
13, 14) Routing from shield to PE kept short to avoid disturbances.
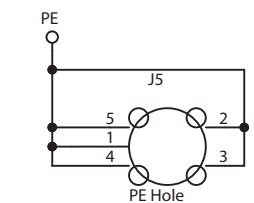
Design Example
PROFIBUS
Network Interface
with D-sub connector

Design Example
PROFIBUS
Network Interface
with M12 connectors

J1

1 — 3V3
2
3 — B_1P/RXP
4 — B_1CEN/SDA
5 — B_1N/RXN
6
7 — B_2P/SDP
8 — B_2CEN/SCL
9 — B_2N/SDN
10
11 — B_3P/TXEN
12 — B_3CEN/RX
13 — B_3N/TXDIS
14
15 — B_4P/TXP/TX
16 — B_4CEN/CD/BUSP_N
17 — B_4N/TXN/TX_N
18
19 — NW_LED4B_N
20 — NW_LED4A_N
21 — NW_LED3B_N
22 — NW_LED3A_N
23 — NW_LED2B_N
24 — NW_LED2A_N
25 — NW_LED1B_N
26 — NW_LED1A_N
27 — 3V3
28
29 — A_1P/RXP
30 — A_1CEN/SDA
31 — A_1N/RXN
32
33 — A_2P/SDP
34 — A_2CEN/SCL
35 — A_2N/SDN
36
37 — A_3P/TXEN
38 — A_3CEN/RX
39 — A_3N/TXDIS
40
41 — A_4P/TXP/TX
42 — A_4CEN/CD/BUSP_N
43 — A_4N/TXN/TX_N
44
45 — C_TX
46 — C_RX
47 — C_TXEN
48 — C_BUSP_N
49 — GATE1
50 — GATE2
51 — 3V3
52

B40-1 connector

R1 220R

U2
Optocoupler
HCPL0601

ISO_5V

RN1C 1k2   RN1D 1k2

U1A
Universal gate
LVC1G97

ISO_GND

ISO_TXEN

U4
CMOS optocoupler
ACPL-077L

3V3   ISO_5V

8 VDD2   VDD1 1
6 OUT   IN 2   ISO_RX
7 NU   NC 3
5 GND2   GND1 4

ISO_GND

U3
1 R   A 6   B
2 RE   B 7   A
3 DE   VCC 8
4 D   GND 5

ISO_5V
ISO_GND

RS-485 transceiver
65HVD1176

RN1A 1k2

ISO_GND

Note that the PROFIBUS
definition of signals A and B
are opposite to the transceiver.

C_RX

U5
CMOS optocoupler
ACPL-077L

3V3

1 VDD1   VDD2 8
2 IN   OUT 6   ISO_TX
3 NC   NU 7
4 GND1   GND2 5

ISO_5V

C_TX

ISO_GND

L3 100nH
L4 100nH

JP2
Male 5 pin B-coded M12 connector
FE

L6 100nH
L5 100nH

JP1
Female 5 pin B-coded M12 connector
ISO_5V
ISO_GND
FE

TR1
1:2.1 Trafo

3V3

Q1 20V/0.4A
Q2 20V/0.4A

GATE1

GATE2

R6 2k2

R7 2k2

C13 10uF/10V
C14 100nF/16V

D1 BAT54C

C10 100nF/16V
C11 1uF/16V

U7
LDO
MIC5207-5.0YM5
IN OUT
Enable Bypass GND

ISO_5V

C12 10uF/10V

ISO_GND

FE
C1 2,2nF/500V
R5 1M
ISO_GND

3V3
U4   U5
C7 100nF/16V   C8 100nF/16V

ISO_GND

ISO_5V
U4   U5   U3   U2
C3 100nF/16V C4 100nF/16V C5 100nF/16V C6 100nF/16V

ISO_GND

ISO_5V
C2 100nF/16V

U1B
VCC#1
VCC
GND
GND#3
Universal gate
LVC1G97

ISO_GND

Design Example
DeviceNet
Network Interface
with open style connector

J1

1 — 3V3
2
3 — B_1P/RXP
4 — B_1CEN/SDA
5 — B_1N/RXN
6
7 — B_2P/SDP
8 — B_2CEN/SCL
9 — B_2N/SDN
10
11 — B_3P/TXEN
12 — B_3CEN/RX
13 — B_3N/TXDIS
14
15 — B_4P/TXP/TX
16 — B_4CEN/CD/BUSP_N
17 — B_4N/TXN/TX_N
18
19 — NW_LED4B_N
20 — NW_LED4A_N
21 — NW_LED3B_N
22 — NW_LED3A_N
23 — NW_LED2B_N
24 — NW_LED2A_N
25 — NW_LED1B_N
26 — NW_LED1A_N
27 — 3V3
28
29 — A_1P/RXP
30 — A_1CEN/SDA
31 — A_1N/RXN
32
33 — A_2P/SDP
34 — A_2CEN/SCL
35 — A_2N/SDN
36
37 — A_3P/TXEN
38 — A_3CEN/RX
39 — A_3N/TXDIS
40
41 — A_4P/TXP/TX
42 — A_4CEN/CD/BUSP_N
43 — A_4N/TXN/TX_N
44
45 — C_TX
46 — C_RX
47 — C_TXEN
48 — C_BUSP_N
49 — GATE1
50 — GATE2
51 — 3V3
52

B40-1 connector

3V3
R1
2k2

3V3
U1
1 VDD1   VDD2 8   ISO_5V
2 IN   OUT 6   ISO_TX
3 NC   NU 7
4 GND1   GND2 5
CMOS optocoupler
ACPL-077L
C_TX
ISO_GND

3V3
R2
2k2

R3
560R
U3
C_BUSP_N
4   1   ISO_5V
3   2
Optocoupler
HCPL-181
ISO_GND

ISO_5V   V+_BUS V-_BUS
U2
1 TXD   VCC 3
4 RXD   CAN_L 6
5 REF   CAN_H 7
8 RS   GND 2
CAN transceiver
65HVD251
ISO_GND

JP4
V-
1 CAN_L
2 SHIELD
3 CAN_H
4 V+
5
DeviceNet connector

R4   C1   RV1
1M   10nF/1kV 30V MOV
FE

3V3
U4
8 VDD2   VDD1 1   ISO_5V
6 OUT   IN 2   ISO_RX
7 NU   NC 3
5 GND2   GND1 4
CMOS optocoupler
ACPL-077L
C_RX
ISO_GND

3V3
U4   U1
C5   C6
100nF/16V 100nF/16V

ISO_5V
U1   U4   U3
C2   C3   C4
100nF/16V 100nF/16V 100nF/16V
ISO_GND

Mind that U5 will
dissipate up to 1.1W
U5
Linear voltage regulator   ISO_5V
7805
V+_BUS
T1
PNP 40V/200mA
2   3   V+_Q   1 IN OUT 3
R5   GND
1k   C9
C7   C8   4   1uF/16V
10uF/50V 330nF/50V
D1
R6
V-_BUS   10k   1A/40V   ISO_GND

Design Example
DeviceNet
Network Interface
with M12 connectors

J1

1 — 3V3
2
3 — B_1P/RXP
4 — B_1CEN/SDA
5 — B_1N/RXN
6
7 — B_2P/SDP
8 — B_2CEN/SCL
9 — B_2N/SDN
10
11 — B_3P/TXEN
12 — B_3CEN/RX
13 — B_3N/TXDIS
14
15 — B_4P/TXP/TX
16 — B_4CEN/CD/BUSP_N
17 — B_4N/TXN/TX_N
18
19 — NW_LED4B_N
20 — NW_LED4A_N
21 — NW_LED3B_N
22 — NW_LED3A_N
23 — NW_LED2B_N
24 — NW_LED2A_N
25 — NW_LED1B_N
26 — NW_LED1A_N
27 — 3V3
28
29 — A_1P/RXP
30 — A_1CEN/SDA
31 — A_1N/RXN
32
33 — A_2P/SDP
34 — A_2CEN/SCL
35 — A_2N/SDN
36
37 — A_3P/TXEN
38 — A_3CEN/RX
39 — A_3N/TXDIS
40
41 — A_4P/TXP/TX
42 — A_4CEN/CD/BUSP_N
43 — A_4N/TXN/TX_N
44
45 — C_TX
46 — C_RX
47 — C_TXEN
48 — C_BUSP_N
49 — GATE1
50 — GATE2
51 — 3V3
52

B40-1 connector

3V3
R1 2k2
C_TX

U1
1 VDD1   VDD2 8
2 IN   OUT 6   ISO_TX
3 NC   NU 7
4 GND1   GND2 5
CMOS optocoupler
ACPL-077L
3V3   ISO_5V
ISO_GND

3V3
R2 2k2
C_BUSP_N

R3
560R
0603

U3
4   1
3   2
Optocoupler
HCPL-181
ISO_5V
ISO_GND

U2
1 TXD   VCC 3   ISO_5V
4 RXD   CAN_L 6
5 REF   CAN_H 7
8 RS   GND 2
CAN transceiver
65HVD251
ISO_GND

V+_BUS

JP2
SHIELD 1
V+ 2
CAN_L 5
V- 3
CAN_H 4
SHIELD 6
Male 5 pin A-coded M12 connector

JP1
V+ 2
SHIELD 1
CAN_L 5
CAN_H 4
V- 3
SHIELD 6
Female 5 pin A-coded M12 connector

V-_BUS

The female connector is optional,
enables daisy chain topology

C_RX
U4
8 VDD2   VDD1 1   ISO_5V
6 OUT   IN 2   ISO_RX
7 NU   NC 3
5 GND2   GND1 4
CMOS optocoupler
ACPL-077L
3V3   ISO_GND

3V3
U4   U1
C5   C6
100nF/16V 100nF/16V
ISO_GND

ISO_5V
U1   U4   U3
C2   C3   C4
100nF/16V 100nF/16V 100nF/16V
ISO_GND

R4
1M
C1
10nF/1kV
RV1
30V MOV
FE

Mind that U5 will
dissipate up to 1.1W
U5
Linear voltage regulator
7805

V+_BUS

T1
PNP 40V/200mA

R5
1k

V+_Q

2 3   1 IN   OUT 3   ISO_5V
GND
C7
10uF/50V
C8
330nF/50V
4
C9
1uF/16V

1

D1
R6
10k
1A/40V

V-_BUS   ISO_GND

Design Example
CC-Link Network Interface

J1

1 3V3
2
3 B_1P/RXP
4 B_1CEN/SDA
5 B_1N/RXN
6
7 B_2P/SDP
8 B_2CEN/SCL
9 B_2N/SDN
10
11 B_3P/TXEN
12 B_3CEN/RX
13 B_3N/TXDIS
14
15 B_4P/TXP/TX
16 B_4CEN/CD/BUSP_N
17 B_4N/TXN/TX_N
18
19 NW_LED4B_N
20 NW_LED4A_N
21 NW_LED3B_N
22 NW_LED3A_N
23 NW_LED2B_N
24 NW_LED2A_N
25 NW_LED1B_N
26 NW_LED1A_N
27 3V3
28
29 A_1P/RXP
30 A_1CEN/SDA
31 A_1N/RXN
32
33 A_2P/SDP
34 A_2CEN/SCL
35 A_2N/SDN
36
37 A_3P/TXEN
38 A_3CEN/RX
39 A_3N/TXDIS
40
41 A_4P/TXP/TX
42 A_4CEN/CD/BUSP_N
43 A_4N/TXN/TX_N
44
45 C_TX
46 C_RX
47 C_TXEN
48 C_BUSP_N
49 GATE1
50 GATE2
51 3V3
52

C_TX
C_RX
C_TXEN

U1 ACPL077L
3V3 VDD1 1 | 8 VDD2 ISO_5V
IN 2 | 6 OUT
NC 3 | NU
GND1 4 | 5 GND2 ISO_GND

U3 ACPL077L
3V3 VDD2 8 | VDD1 1 ISO_5V
OUT 6 | IN 2
NU 7 | NC 3
GND2 5 | GND1 4 ISO_GND

U4 ACPL077L
3V3 VDD1 1 | 8 VDD2 ISO_5V
IN 2 | 6 OUT
NC 3 | NU 7
GND1 4 | 5 GND2 ISO_GND

U2 65HVD1176
DI 4 | 8 VCC ISO_5V
RO 1 | 6 A
DE 3 | 7 B
RE 2 | 5 GND ISO_GND

L2 0R
L3 0R
L1
MCT7050-A4

J4 MSTBA
DA 1
DB 2
DG 3
SLD 4
FG 5

C1 3,3nF/50V
PE

U5A LVC1G97-14
C_TXEN 6 | 4

R3 2k2
R5 2k2
R4 10k
R6 10k

U6A LVC1G97-14
6 | 4

ISO_GND

PE
J3
2 | 5
1
3 | 4

Q1 Si1062X
Q2 Si1062X
R1 2k2
R2 2k2
GATE1
GATE2

3V3
TR1 1:2.1 trafo
1 | 6
2 | 5
3 | 4

C6 10uF/10V
C5 100nF/16V

D1 BAT54C
C4 100nF/16V
C3 1uF/16V

U7 MIC5207
IN 1 | OUT 5 ISO_5V
Enable 3 | Bypass
GND 2
C2 10uF/10V
ISO_GND

ISO_5V
^`mi MITi Er NF C7 100nF/16V
^`mi MITi Er PF C8 100nF/16V
^`mi MITi Er QF C9 100nF/16V
SRes aNNTS Er OF C10 100nF/16V

U6B LVC1G97-14
VCC#1 | VCC 1
GND | 5
GND#3
C13 100nF/16V
ISO_GND

3V3
^`mi MITi = Er NF C11 100nF/16V
^`mi MITi Er PF C12 100nF/16V
^`mi MITi Er QF C14 100nF/16V

U5B LVC1G97-14
VCC#1 | VCC 1
GND | 5
GND#3
C15 100nF/16V

Design Example
CANopen
Network Interface

ISOLATION AREA HOST   ISOLATION AREA NETWORK

J1

B40-1 connector

1	3V3
3	B_1P/RXP
4	B_1CEN/SDA
5	B_1N/RXN
7	B_2P/SDP
8	B_2CEN/SCL
9	B_2N/SDN
11	B_3P/TXEN
12	B_3CEN/RX
13	B_3N/TXDIS
15	B_4P/TXP/TX
16	B_4CEN/CD/BUSP_N
17	B_4N/TXN/TX_N
19	NW_LED4B_N
20	NW_LED4A_N
21	NW_LED3B_N
22	NW_LED3A_N
23	NW_LED2B_N
24	NW_LED2A_N
25	NW_LED1B_N
26	NW_LED1A_N
27	3V3
29	A_1P/RXP
30	A_1CEN/SDA
31	A_1N/RXN
33	A_2P/SDP
34	A_2CEN/SCL
35	A_2N/SDN
37	A_3P/TXEN
38	A_3CEN/RX
39	A_3N/TXDIS
41	A_4P/TXP/TX
42	A_4CEN/CD/BUSP_N
43	A_4N/TXN/TX_N
45	C_TX
46	C_RX
47	C_TXEN
48	C_BUSP_N
49	GATE1
50	GATE2
51	3V3

C_TX
C_RX
GATE1
GATE2

3V3
RN1A
2k2

U8
CMOS optocoupler
ACPL077L

1	VDD1	VDD2	8
2	IN	OUT	6
3	NC	NU	7
4	GND1	GND2	5

3V3   ISO_5V
ISO_GND

TP7
CAN_TXD
test_smd_35

U9
CAN transceiver
65HVD251

1	TXD	VCC	3
4	RXD	CAN_L	6
5	REF	CAN_H	7
8	RS	GND	2

ISO_5V
ISO_GND

JP5
DSUB9-male

1	
6	
2	CAN_L
7	CAN_H
3	ISO_GND
8	
4	
9	
5	SHIELD
10	
11	

U11
CMOS optocoupler
ACPL077L

8	VDD2	VDD1	1
6	OUT	IN	2
7	NU	NC	3
5	GND2	GND1	4

3V3   ISO_5V
ISO_GND

TP8
CAN_RXD
test_smd_35

ISOLATION AREA FE

RV1
V30MLA1812TX1884
C40
10nF/1kV
R55
1M
FE

Q1
20V/0.4A
Q2
20V/0.4A

RN1B
2k2

RN1C
2k2

3V3

TR1   1:2.1 Trafo

1	6
2	5
3	4

D5
Schottky diode
BAT54C

C49
NM(100nF/16V)
C50
1uF/16V

U13
5V LDO
MIC5207

| 1 | IN | OUT | 5 |
| 3 | Enable | Bypass GND | |

C51
4,7uF/6,3V
R52
680R

ISO_5V
ISO_GND

C52
10uF/10V

RN1D
2k2
0603_8P

3V3

U8 ACPL077L   U11 ACPL077L

C41
100nF/16V
C42
100nF/16V

ISO_GND

ISO_5V

U8 ACPL077L   U9 65HVD251   U11 ACPL077L

C43
100nF/16V
C45
100nF/16V
C53
100nF/16V

ISO_GND

NOTES:
1) Discharge resistor