Hardware Implementation Example
Anybus CompactCom M40 16 bit mode
STM32F407Z

History

Revision	Date	Description	Responsible
0.99	2014-11-03	First draft	joka
1.00	2015-06-08	First official version	Joka, kel

Contents

1 Requirements

Hardware
Anybus CompactCom M40
STM32F407Z ARM MCU
74LVC32, OR-gate (or similar)

Documentation	Document number	Version
Anybus CompactCom M40 Hardware Design Guide	HMSI-216-126	1.31
Reference manual RM0090: TM32F405xx/07xx, STM32F415xx/17xx, STM32F42xxx and STM32F43xxx advanced ARM®-based 32-bit MCUs	18909	7

2 Solution Overview

This is a description of how to design for Anybus CompactCom M40 with 16-bit parallel mode when using the STM32 MCU STM32F407Zx with FSMC(flexible static memory controller). The FSMC_A[0] should be connected to the lowest address bit of the Anybus CompactCom. When the Anybus CompactCom is configured for 16 bit mode input A0 of the Anybus CompactCom is not used as address input but as /WE input for the high byte. The lowest address input for addressing a 16 bit value is A1. How the hardware signals shall be connected can be seen in Figure 1.

This is a complement to the Anybus CompactCom M40 Hardware Design Guide.

2.1 Reference information from STM32 Datasheet

Table 210. External memory address

Memory width(1)	Data address issued to the memory	Maximum memory capacity (bits)
8-bit	HADDR[25:0]	64 Mbytes x 8 = 512 Mbit
16-bit	HADDR[25:1] >> 1	64 Mbytes/2 x 16 = 512 Mbit

1. In case of a 16-bit external memory width, the FSMC will internally use HADDR[25:1] to generate the address for external memory FSMC_A[24:0].
Whatever the external memory width (16-bit or 8-bit), FSMC_A[0] should be connected to external memory address A[0].

Table 216. Nonmultiplexed I/Os PSRAM/SRAM

FSMC signal name	I/O	Function
CLK	O	Clock (only for PSRAM synchronous access)
A[25:0]	O	Address bus
D[15:0]	I/O	Data bidirectional bus
NE[x]	O	Chip select, x = 1..4 (called NCE by PSRAM (Cellular RAM i.e. CRAM))
NOE	O	Output enable
NWE	O	Write enable
NL(= NADV)	O	Address valid only for PSRAM input (memory signal name: NADV)
NWAIT	I	PSRAM wait input signal to the FSMC
NBL[1]	O	Upper byte enable (memory signal name: NUB)
NBL[0]	O	Lowed byte enable (memory signal name: NLB)

3 Application Note

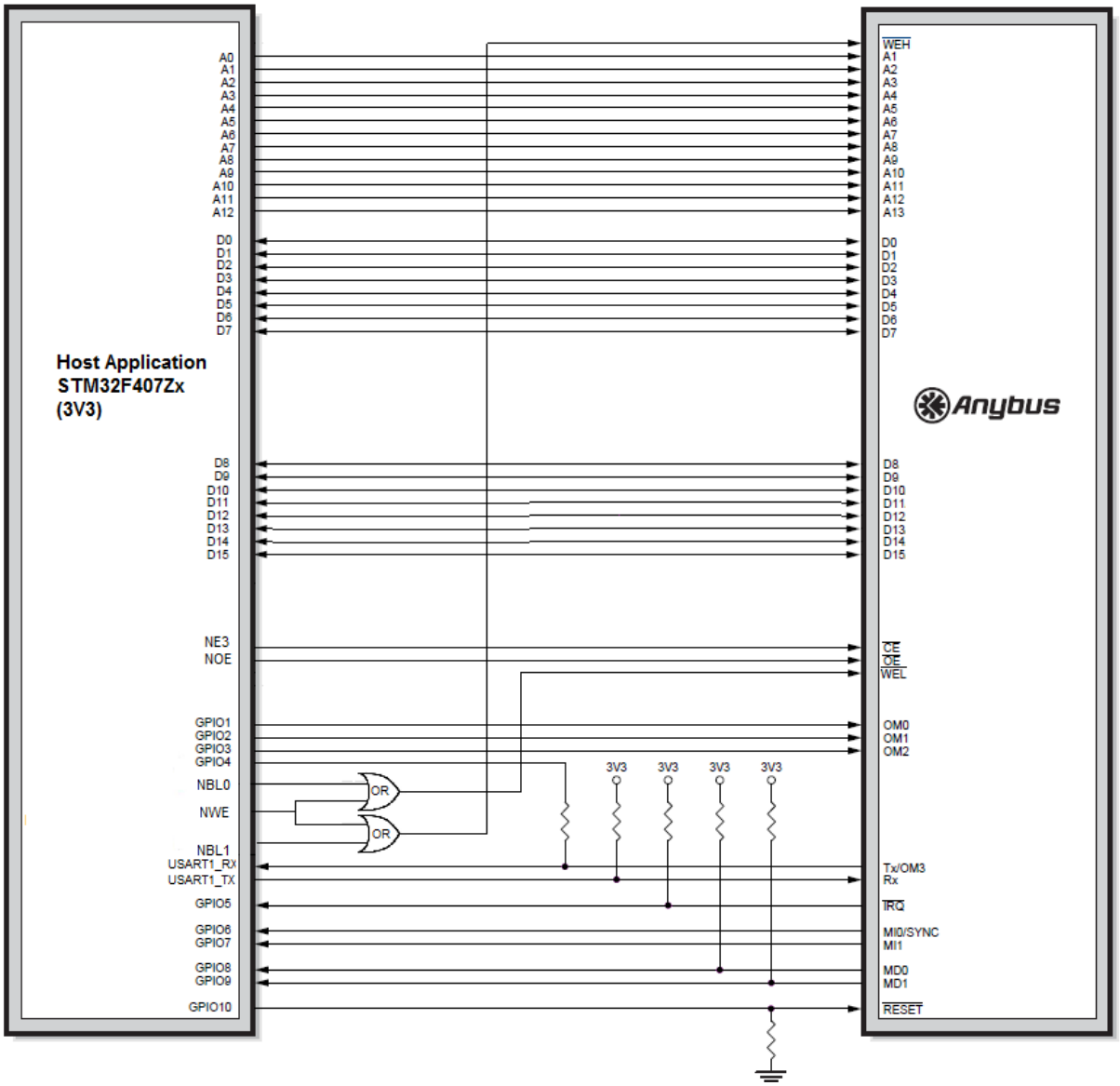

Figure 1 Hardware implementation example of using the Anybus CompactCom in 16 bit mode connected to an STM32F407Z

4 More Information about the Network and Products

The latest manuals, can be found on HMS homepage, www.anybus.com.